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PRODUCT RESOURCE GUIDE

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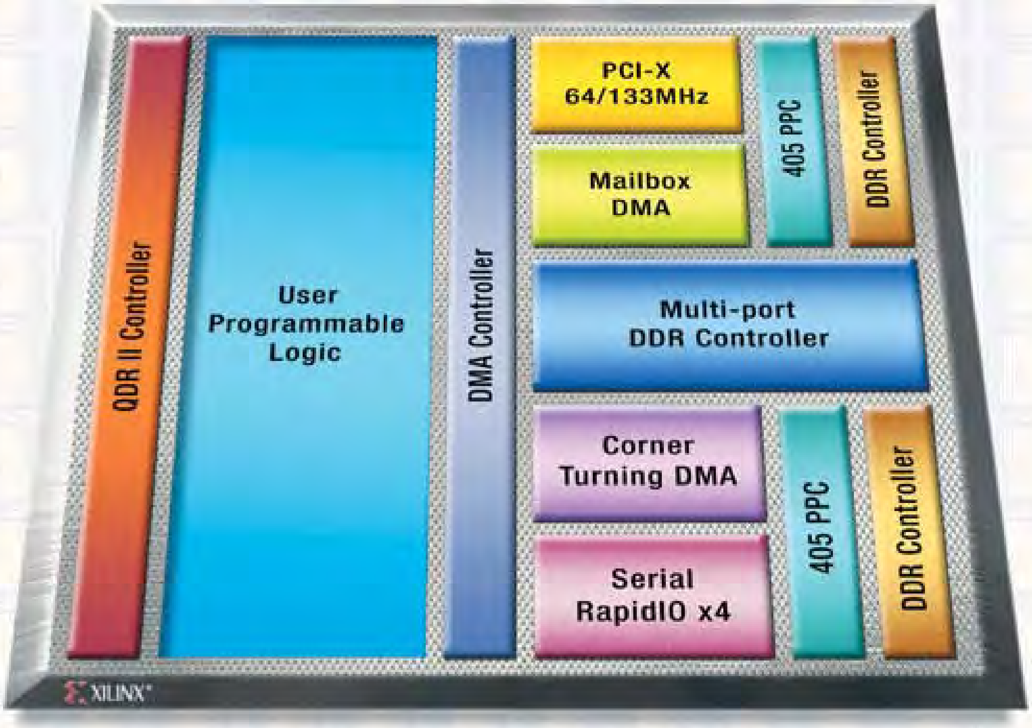

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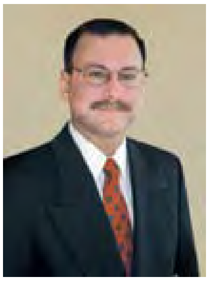
Editor’s Foreword



2nd Annual DSP-FPGA.com Product Resource Guide 2005

By Chris Ciufo

Welcome to the second annual *DSP-FPGA.com Product Resource Guide*. Inside you’ll find the information you need to evaluate, specify, design, and deploy an FPGA- or DSP-based system. We see tomorrow’s systems as being a mixture of both types of devices. So, we’ve worked with the industry’s best and most popular vendors and suppliers to organize and present to you technical information in an easy-to-read and even easier to search resource tool. Here you’ll find technology ranging from carrier boards, FPGA and DSP devices, data acquisition products, and products such as software and IDE tools as well. No matter your favorite architecture or IC vendor, you’re likely to find related products in this resource guide.

DSPs and FPGAs represent one part of the embedded industry that’s in full-scale growth mode. In FPGAs alone, integrated circuit vendors, for example, are introducing devices with unheard of densities and unbelievable onboard resources. For instance, new product offerings in the last twelve months just from Altera, Lattice, and Xilinx show that non-linear innovation is leapfrogging incremental improvements. Architectures such as the Virtex-4 platform approach with multi-gigabit LVDS interfaces, rad-tolerant FPGAs from Actel, and low-cost Cyclone II offerings from Altera show the FPGA edging out ASICs and ASSPs in all but the highest volume applications.

New IP instantiations, from the IC vendors themselves and from a growing cadre of third-party vendors, mean users often don’t have to design their own logic – preconfigured “soft” logic blocks represent already-designed complete subsystems such as Micro Memory’s CoSine FPGA-based DSP memory controller/accelerator/bus bridge. This type of soft IP is complementing hardwired “hard” IP; these are logic blocks already fixed in silicon such as PowerPC and ARM microprocessor cores. Indeed, the FPGA has become the System-on-Chip (SoC) of choice for today’s designers.

In addition, FPGAs are destined to coexist with the latest DSP processors from Texas Instruments and Analog Devices, as increasingly “logic-aware” operating systems can make on-the-fly decisions about which computational resources to use: logic on the DSP, on the FPGA’s pool of gates, or the hard-wired logic blocks on the FPGA. Increasingly, systems will use *all three*, moving towards intelligent reconfigurability that scales and adapts to solving tomorrow’s most challenging computational, communications, and signal processing problems.

We hope you enjoy this second annual *DSP-FPGA.com Product Resource Guide*. We’ve sure enjoyed compiling this information for your benefit.

Please be sure to check out the interactive version of this resource guide at: www.dsp-fpga.com

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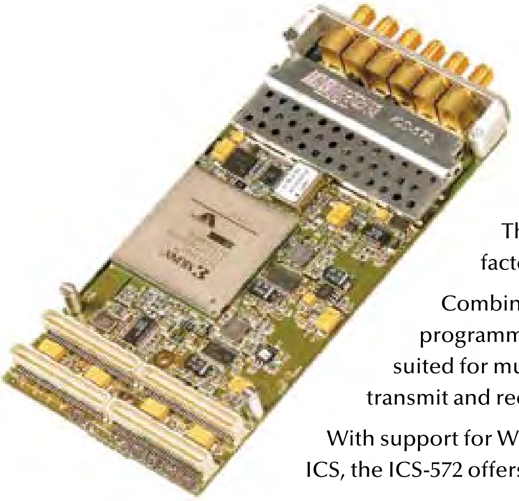

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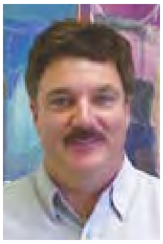
Digital signal controller applications



By Venkat Anant, Senior Staff Applications Engineer, and
Bill Hutchings, Senior Systems Engineer,
Freescale Semiconductor Digital Signal Controller Operation

In an increasingly competitive market driven by cost and time-to-market requirements, designers have been using low-cost microcontrollers in their embedded systems. Engineers designed these processors to control entire systems, including all the supervisory tasks, in addition to handling user interfaces. Having limited processing power, these microcontrollers could execute only simple control algorithms, thus limiting their functionality. DSPs, on the other hand, are number crunching devices typically suitable for high-end applications such as telecommunications and audio/video processing, which require a lot of processing in a short amount of time. However, they do not have the control capabilities of microcontrollers.

Using the DSP as a coprocessor became a natural, progressive step when designing embedded systems requiring signal processing capabilities. It strictly implemented the control algorithm while the microcontroller managed all other tasks. Although this processor marriage was functional, manifold problems associated with such a design evolved. The handshaking required in a two-processor solution resulted in wasted machine cycles that ate into the design margin allocated for application feature enhancements and bug fixes. The system required a high-speed communication path to ferry a significant amount of data back and forth. Perhaps the most significant problem of all was that the design cycle time greatly increased due to the learning curve and integration between the two processors. After factoring in production and manufacturing issues, a two-processor solution proved to be more time consuming, as well as costly.

The solution

A single chip that incorporates the advantages of microcontrollers and DSPs clearly provides the preferred solution. A Digital Signal Controller (DSC) can execute both efficient digital signal processing and a variety of controller operations in a single chip. By combining the processing power of a DSP with the programming simplicity of a microcontroller, a DSC can provide high-speed, low-cost, and easy-to-design solutions. As a result, DSCs have taken away some of the microcontroller market share because they provide the best of both worlds.

Figure 1 depicts a typical type of architecture and system integration that one such DSC by Freescale provides. The basis of the core, a dual Harvard-style architecture, consists of three execution units that operate in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

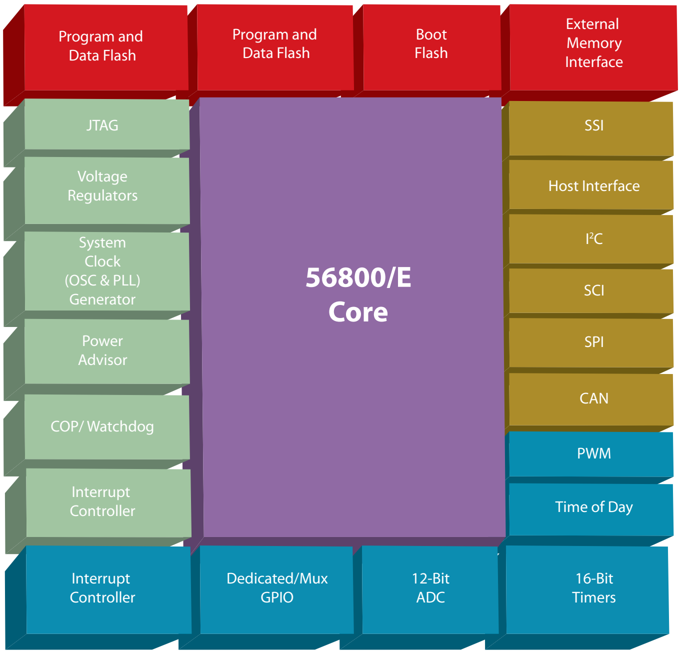


Figure 1

In addition, a variety of peripherals enhances performance, reduces applications cost, and promotes ease of product development. The blocks in red show the available on-chip and off-chip memory configuration options. On-chip Flash enables true standalone system development as no need for external memory to operate exists. The blocks in gold show the communication options available for inter-processor communication as well as off-chip peripheral integration. The blocks in blue show general-purpose peripherals typically found in microcontrollers. The blocks in green show dedicated resources required for safe operation as well as cost savings by not requiring external circuitry for system debugging, power supervision, voltage regulation, and system reset.

A sensorless Field Oriented Control (FOC) of a three-phase AC Induction Motor is a good example for understanding how DSCs can provide this flexibility and cost savings.

Control of AC Induction Motors (ACIM)

DSCs provide the capability to replace the analog circuitry of traditional designs with digital signal processing, which creates a significant advantage. Examples include:

- Replacing analog filters with digital filters
- Replacing complex universal motors with a combination of a simpler motor type and more complex digital control algorithms
- Replacing power control circuitry with digital control algorithms that work in conjunction with PWM/ADC feedback loops

One can easily see how this type of replacement can lead to overall system cost reduction as well as flexibility in design. The lifetime of the hardware target system design is greatly extended, and feature enhancement, bug correction, and field upgrades can be made in software as opposed to hardware replacement.

Traditionally, the costs of implementing the control and power stage hardware have slowed three-phase motors' use of FOC for price-sensitive applications. But new advances in Flash-based DSCs and power modules have greatly reduced these costs. Figure 2 shows a high-level implementation of the control and power stage circuitry. Advances in power drivers and DSCs have greatly simplified and reduced the cost of the design. The DSC has all the capability required to perform the complete motor control functions digitally. Flash memory internally stores the firmware, as well as the data needed for running the application. The DSC also has internal peripherals such as the PWM, ADC, I2C, SCI/SPI, GPIO, and an on-chip relaxation oscillator, making it a very integrated solution.

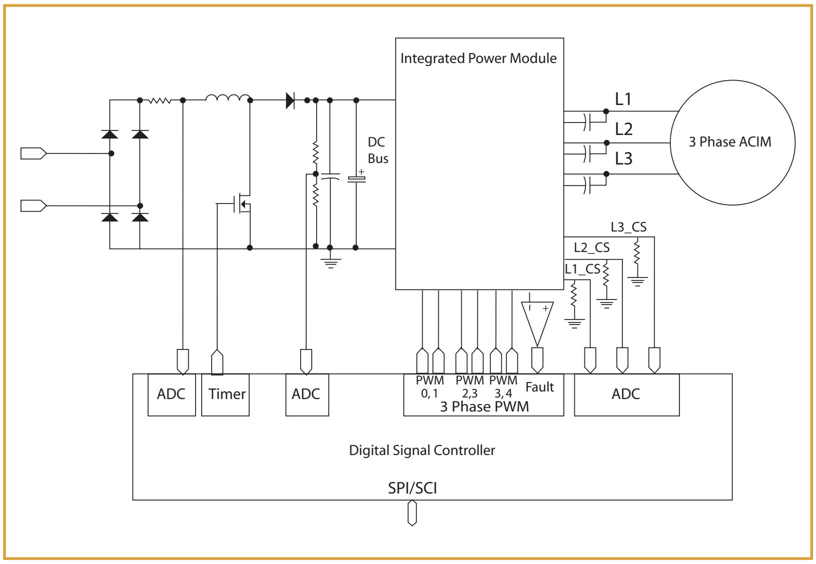


Figure 2

Since the DSC executes digital signal processing algorithms and MCU tasks efficiently, it is capable of running the computationally intensive FOC algorithms. This one low-cost part can replace what previously had to be performed with several expensive components such as a PWM controller, FPGA or DSP, ADC, PFC controller, crystal oscillator, and other support and safety circuitry.

The front-end circuitry performs the rectification as well as the power factor correction under the control of the DSC. The DC signal is fed into the integrated power module, which has the power devices configured as an H-bridge that are controlled via the PWM peripheral on the DSC. The output from the IPM comprises three phase sinusoids that are connected into the ACIM motor. The IPM also has outputs used for current sensing for each leg of the motor and are input into the DSC's ADC inputs. The IPM has a temperature sense capability, so an over-temperature condition can be fed into the fault input of the PWM peripheral as shown in the figure. In addition, other safety critical errors, such as overcurrent and overvoltage conditions, can be fed into individual fault inputs on the PWM peripheral. The PWM peripheral can be configured to have these fault inputs turn off the PWM outputs, thereby turning off the IPM power devices and halting the error condition that could cause physical or bodily damage. These features again eliminate external circuitry.

The sensorless FOC algorithm does not require position or speed sensors to simplify and lower the system cost. With DSCs, computationally intensive coordinate transformations can be executed on the fly giving excellent dynamic control. In addition, excellent torque control with the FOC control simplifies the mechanical transmission to a direct drive method.

The significantly simplified system greatly enhances system reliability while providing superior performance. Parts count has been reduced. Simpler and more reliable ACIM motors and transmission systems can be used. The manufacturing process can also be streamlined and enhanced. Since the features and capability of the motor control can be modified through software, the same system can be used for many different models and provides the benefits of scale. Since the DSC is Flash-based, the specific software can be programmed into the device at the time of board manufacture or afterwards, enabling a significant logistics advantage in flexible manufacturing.

The importance of a single-chip DSC solution in embedded applications cannot be overemphasized. Such a high-performance core with a comprehensive set of peripherals provides a formidable solution suited to a variety of applications. DSCs offer design flexibility and increased efficiency while keeping down costs and reducing time to market, which poses the question: How can your design benefit by using a DSC?

For more information, visit the Freescale website at www.freescale.com.

When MCUs and DSPs Collide: Digital Signal Controllers

By Sumit Mitra, Vice President,
Digital Signal Controller Division, Microchip Technology Inc.

Microcontrollers (MCUs) and Digital Signal Processors (DSPs) have historically suited different application categories. The vast majority of DSPs are used in baseband wireless communication applications, whereas MCUs are used in a wide variety of applications. Embedded engineers now seeking the benefits of digital signal processing in traditional MCU applications now have a new choice.

A Digital Signal Controller (DSC) is an embedded controller that seamlessly integrates the algorithm processing power of a DSP engine with the hard, real-time control abilities of a microcontroller. A DSC has the easy-to-use look and feel, peripheral complement, and nonvolatile memory attributes of an MCU, yet the power of a DSP.

Microchip coined the term DSC publicly in 2002, when it became evident that the convergence of the traditional MCU and DSP space was emerging as a new market space.

The blending of an MCU and DSP is an art unto itself (see Table 1 for a list of MCU, DSP, and DSC attributes). Microcontrollers thrive on interrupts; DSPs avoid them. The prime driver for MCUs is real-time control and deterministic response. The prime driver for DSPs is performance. MCUs typically offer a single-chip solution; DSPs often require external memory, an FPGA, a controller, and other glue logic. Microcontrollers are programmed in C; DSPs of this category typically use assembly language.

Attribute	MCUs	DSPs	DSCs
Execute From Flash	x		x
Large Register Set	x		x
Robust Interrupt Capability	x		x
Abundant Mixed Signal	x		x
Single-Cycle MAC		x	x
Dual-Operand Fetch		x	x
Zero-Overhead Loops		x	x
Saturation/Rounding		x	x
Bit-Reverse Modes		x	x

Table 1

Motor control – specifically, the desire to obtain faster motor speeds, respond more accurately to changes of load, or reduce motor cost – initially drove the DSC market. The initial DSC market driver was motor control – to obtain faster motor speeds, respond more accurately to changes of load or reduce motor cost. As motor control devices became available, myriad other applications discovered the benefit of the unique technology combination. The next wave was traditional analog applications flooded the market next, replacing multi-loop configurations and analog filters with digital implementations. The third wave included those replacing multiple chips to achieve cost or size reduction. As these waves of customer activity became apparent, makers of MCUs and DSPs rushed to address this emerging market space.

> **"The DSC is beginning to emerge as its own market segment, just as the microcontroller evolved from the microprocessor into its own product category."**

Some MCU manufacturers simply added Multiply Accumulate (MAC) functionality to MCUs. But there is a lot more to a DSP processor than a simple MAC. Channeling data in and out of a high-speed DSP engine, handling various data types, dealing with saturation and overflow during computation, and addressing modes specific to DSP algorithms are some of many attributes that designers cannot simply "slap on" to an existing MCU. Thus, these products failed to match DSPs' performance when executing real-life algorithms.

Conversely, some DSP suppliers added MCU-style peripherals around a DSP to achieve the same goal. Such controllers, built out of DSP cores, lack essential control features such as fast and deterministic interrupt response or bit-manipulation capabilities.

The best solutions were developed from the ground up, taking into account the complexities of both the DSP and MCU worlds.

Semiconductor market impact

The impact of DSCs is already visible in the semiconductor market. Users are demanding a DSC that can do it all – rather than settling for having to use a separate DSP and an MCU. With easy-to-use DSCs, users can add more DSP features into traditional control applications such as voice commands, speech compression/playback, embedded modems, encryption, pattern recognition, and so on. Vendors, having recognized DSC as a rapidly emerging market segment, are introducing more products.

The need for more memory, not high performance, is what originally drove the 16-bit MCU market. Therefore, most 16-bit MCUs meet this requirement. DSCs are pushing the performance front in the controller market.

Technology considerations

Traditionally, MCU manufacturers have used mature lithography to achieve lower cost. DSP manufacturers, on the other hand, use leading-edge lithography to achieve higher performance. The technology selection of DSCs is not as straightforward. Integrating Flash program memory and analog peripherals is essential for DSC applications. Thus, technology must support the required logic, speed, analog, and Flash integration (see Table 2).

With tighter lithography
Operating Power Declines
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Core Voltage Decreases
Mixed-Signal Options Become Challenging/Expensive
High Voltage Capability Becomes Expensive
Multiple Supply Voltages or Regulators are Needed
Flash Endurance Declines
Die Size Decreases (except analog)
Wafer Cost Increases

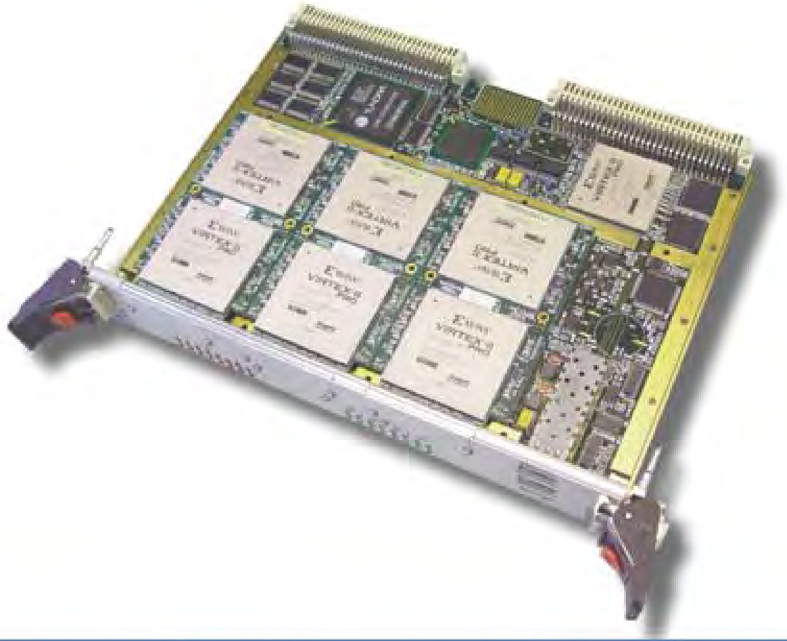
Table 2

As a long-time leading supplier of field-programmable, analog-rich microcontrollers, Microchip had no difficulty in reaching into the DSC product arena.

Microchip developed the dsPIC® DSC architecture from the ground up to truly integrate the algorithm processing power of a DSP and the real-time control features of an MCU, without any compromise. Codevelopment of the architecture, compiler, and algorithm was instrumental to the successful blending of architectures.

The semiconductor market is ever-changing. The DSC is beginning to emerge as its own market segment, just as the microcontroller evolved from the microprocessor into its own product category. Having pioneered the DSC, Microchip is fully committed to this important, emerging market.

For more information, visit the Microchip website at www.microchip.com.



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FEATURES:

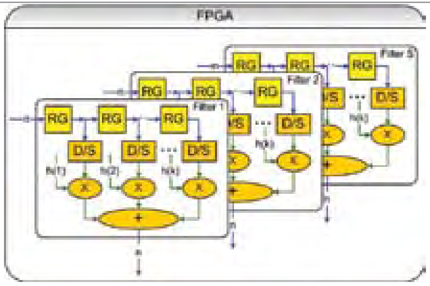
- Clock and synchronize up to 16 channels of 1.5 GSps with 8-bit resolution
- Continuous real-time data collection at up to 24 GSps
- Continuous real-time data processing of full 24 GSps
- Full bandwidth distribution of raw and processed data
- COTS turnkey system – user configurable and scalable
- WILDSTAR II Pro for VME has up to three Xilinx Virtex II Pro 70 or 100 FPGAs
- WILDSTAR II Pro for VME carries one or two I/O cards – up to five FPGAs per slot
- Fibre Channel 2, WILDSTAR data port, GigE, and other I/O available
- Full CoreFire FPGA application support with more than 800 IP cores
- Achieve world-class performance – WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support
- Training classes and application support also available

For more information, contact: wfinfo@ annapmicro.com RSC #1301 @ www.DSP-FPGA.com/catalogrsc

DSP TOP

64 Rockledge Drive
Livingston, NJ 07039
Tel: 973-758-9789 • Fax: 419-818-3002
www.dsptop.com

Digital Filters



DSP TOP announces implementation of their set Digital Filters on a single standalone FPGA. Operation and functions are fully determined by the internal hardware structure. The external connections of a chip are just: clock, DATA_IN, and DATA_OUT.

The FIR filters of DSP TOP are the first products based on the Stochastic Computing principles. The adders and multipliers of all filters compose computing arrays in which every arithmetic unit operates independently, simultaneously, and in parallel.

The frequency response and dynamic range of the filters are defined by h-coefficients, n-bit resolution of DATA, and clock frequency.

FEATURES:

- Number of the filters defined by design
- Every filter operates independently
- Other types of FIR are accepted
- Different types FPGAs are used
- Coefficients of the filter could be modified
- Frequency response covers a range from 0-2 MHz

For more information, contact: dsptop@ dsptop.com
RSC #1401 @ www.DSP-FPGA.com/catalogrsc

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(A member of Radstone Embedded Computing)
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Chantilly, VA 20151
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www.ics-ltd.com

ICS
SENSOR PROCESSING

ICS daqPC

Maintaining its trailblazing performance, the ICS daqPC is now capable of recording and playback of analog signals at an amazing rate of 600 MBps. The two-box solution is 19" rackmountable with a total height of 7U (12.3") providing 2.8 TB of data storage capability. This compact system is incredible for recording high bandwidth signals and as a multichannel arbitrary waveform generator, and has been used in a variety of applications. The daqPC can be very easily configured using ICS ADC/DAC cards to suit a user's exact requirement.

FEATURES:

- Offers high-speed record/playback capability, storing up to 2.8 TB of digital data on an array of hard drives
- Digital recording of sensor signals at over 600 MBps sustained rate
- daqPC supports time-stamp recording using either an on-card or off-card source
- Available in rackmount and portable versions
- Built-in 1 Gb network interface
- NTFS file system for easy post processing of recorded data

For more information, contact: sales@ ics-ltd.com
RSC #1402 @ www.DSP-FPGA.com/catalogrsc

StarCore

Your Source for Embedded Signal Processing

8303 Mopac Expressway, Suite A400
Austin, TX 78759
Tel: 512-682-8558 • Fax: 512-682-8699
www.starcore-dsp.com

SC2000 Family

The StarCore™ SC2000 family is the next generation of processor cores and peripheral Intellectual Property (IP) blocks from StarCore, featuring advanced video-processing performance, enhanced real-time operating system support, and lower power consumption. Based on the leading-edge StarCore V4 architecture, the SC2000-family cores provide more efficient video encoding and decoding in software, reduce power consumption for converging mobile systems, and enable the use of denser, faster compiled code.

Advanced multimedia

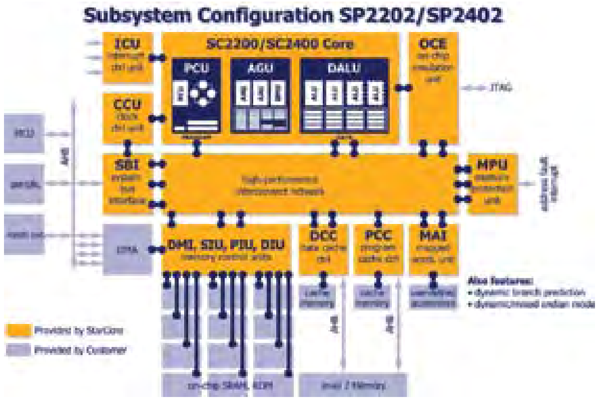
The V4 architecture offers new and enhanced multimedia instructions – including Single Instruction Multiple Data (SIMD) instructions – to provide for the efficient implementation of video algorithms in software. For example, tight motion-estimation loops that take advantage of the new SAD4 instruction execute up to 13 times faster than on the StarCore V2 architecture. As a result, SC2000-family cores can perform simultaneous software encoding and decoding of VGA-quality MPEG-4 video at 30 frames per second and beyond. As an example, CIF (352 x 288-pixel) video encoding at 15 frames per second requires only about 50 MHz, or 10 percent of a 500 MHz StarCore V4 processor's computational capability, while video decoding can be performed with less than 20 MHz. This acceleration of software algorithms increases performance headroom, enabling true single-core systems.

Efficient, compact code

The innovative StarCore Variable Length Execution Set (VLES) architecture provides parallel execution of as many as six instructions for superior performance, with no code size penalty for VLESs that contain fewer instructions. Now, new instructions make StarCore processor cores better compiler targets by improving a compiler's ability to deliver faster, denser compiled code.

StarCore V5 architecture

StarCore's new V5 architecture will be available in October 2005. Visit the StarCore website for more information.



FEATURES:

- Target applications: Mobile multimedia, single-core wireless modem, voice processing; converging consumer devices; wireline
- Powerful, efficient StarCore V4 instruction-set architecture
- 100 percent binary backward compatibility with SC1000-family (V2 architecture)
- Six-stage, balanced pipeline, parallel, six-issue (SC2400)
- VLES architecture, providing high VLIW parallelism and compact code
- Single-cycle execution of most instructions; energy-saving low power mode
- Two (SC2200) or four (SC2400) independent Arithmetic-Logic Units (ALUs)
- Up to two 64-bit data-memory moves per cycle; orthogonal usage of registers
- 40-bit MAC (16-bit multiplier) and Bit-Field Unit (BFU) per ALU
- Two independent Address-Arithmetic Units (AAUs) and one BMU
- Optional fully associative branch target buffer for dynamic branch prediction

For more information, contact: pr@ starcore-dsp.com RSC #1501 @ www.DSP-FPGA.com/catalogrsc

Annapolis Micro Systems, Inc.

Your Source for Embedded Signal Processing

190 Admiral Cochrane Drive, Suite 130
Annapolis, MD 21401
Tel: 410-841-2514 • Fax: 410-841-2518
www.annapmicro.com

Quad Fibre Channel 2

Annapolis Micro Systems is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, digital signal processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications.The Annapolis WILD Quad Fibre Channel 2 card breaks the PCI bottleneck between your input data source and your processing power. Supporting up to 1.6 GBps of incoming data with four full-duplex channels, the card provides four million gates of user reprogrammable FPGA logic for onboard processing. The 4 GBps per I/O card of aggregate bandwidth down to the motherboard provides access to up to 30 million more FPGA gates on a WILDSTAR II Pro for VME motherboard.

Our boards are on a large number of operating systems, including Win (NT, 2000, XP), Linux, DECAlpha, Solaris, IRIX, ALTIX, MacOS, and VxWorks. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. We offer training, including customized application development and customer support. Develop your application very quickly and easily with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily and quickly build and test their algorithms on the real hardware that will be used in the field. CoreFire is based on data flow and automatically generates distributed control fabric between cores. Our extensive IP and board support libraries contain more than 800 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and povides proven, reusable, high-performance IP modules.The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, and dollars.

FEATURES:

- Four full-duplex channels with up to 400 MBps peak data rate per channel
- Up to 1.6 GBps total Fibre Channel 2 I/O per I/O card
- Up to 4 GBps per I/O card total bandwidth down to motherboard
- No bus latency between FC2 I/O data source and processing power
- Full PCI bandwidth from motherboard to PCI host at up to 500 MBps
- Virtex II Xilinx FPGA processing element – XC2V4000-5
- Pluggable replaceable transceivers for maximum technology refresh
- Programmable Flash to store FPGA images and program FPGA on power-up
- Full CoreFire board support package to integrate I/O card into application
- VHDL model, including some source code
- Achieve world-class performance – WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

For more information, contact: wfinfo@ annapmicro.com

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Your Source for Embedded Signal Processing

Dual 1.5 GHz A/D Board

Annapolis Micro Systems is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, digital signal processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications. The Annapolis Dual 1.5 GHz A/D I/O card provides two channels of 1.5 GSps input (with 8-bit resolution) or one channel of 3.0 GSps input (with 8-bit resolution). The board has two Max1088-bit A/D converters, each one fed by its own pair of differential signals. The differential clock signals coming into the board can provide identical clocks to both A/D converters for dual 1.5 GSps channels or an inverted clock to one of the A/D converters to interleave the data for a single 3.0 GSps channel. Multiple I/O cards can be synched together via the Annapolis Clock Sync Distribution Board, as in the 24 GSps A/D converter Collection, Processing and Distribution (CPD) system. The Xilinx Virtex II Pro 70 on the board provides user-configurable, real-time continuous sustained processing of the full data stream. Up to two of these I/O cards can reside on the Annapolis WILDSTAR II or WILDSTAR II Pro FPGA-based VME and PCI bus boards, which provide up to 30 million more user reprogrammable FPGA gates for onboard processing. Our boards run on many different operating systems. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. We offer training, including customized application development and customer support. Developing applications with CoreFire (more than 800 cores) transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. The combination of our COTS hardware and CoreFire lets our customers make massive improvements in processing speed, while achieving savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

FEATURES:

- Two MAX 108 8-bit A/D converters – two 1.5 GSps channels or one 3 GSps channel
- Two sets of differential input signals – one for each A/D converter
- Differential clock input – Synchronize or interleave the two data streams
- Up to 6 GBps I/O bandwidth to WILDSTAR II Pro motherboard I/O slot
- Xilinx Virtex II Pro XC2V70 FPGA for user reprogrammable processing
- Heat sink on FPGA
- Host software: Win NT, 2000, XP, Linux, VxWorks, Solaris, MacOS, DECAlpha, and SGI
- Full CoreFire board support package for fast and easy application development
- VHDL model, including some source code
- Save time and effort and reduce risk with COTS boards and software
- Achieve world-class performance – WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

For more information, contact: wfinfo@ annapmicro.com

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Your Source for Embedded Signal Processing

ICS SENSOR PROCESSING

ICS-572

Providing both receive and transmit capability for demanding radar and communications applications, the ICS-572 PMC module combines industry-leading ADC and DAC technologies with a high-density, high-speed FPGA to offer an efficient combination of cost, size, and performance in a single PMC site.

The ICS-572 PMC includes two 14-bit, 105 MHz ADCs, two 14-bit, 200 MHz DACs, a 4 or 6 M gate Xilinx FPGA, 64 MB SDRAM, 8 MB QDR II SRAM, 64 user programmable I/O via Pn4, and a 64-bit, 66 MHz PCI DMA interface.

ICS-572 is ideally suited for radar, communications, EW, test and measurement, public safety, and so forth.

FEATURES:

- Receive and transmit functions in one single width PMC module
- Ideally suited in high-bandwidth communications applications that require both receive and transmit functions
- Two 14-bit, 105 MHz ADCs, and two 14-bit, 200 MHz DACs
- The board includes a 4 or 6 M gate Xilinx Virtex II user programmable FPGA for baseband processing
- Onboard data storage with 64 MB of SDRAM and 8 MB of QDR II SRAM, and a fast PCI 2.2 64-bit, 66 MHz DMA interface
- Comprehensive software device drivers support the ICS-572 board for the Windows, Linux, and VxWorks operating systems

For more information, contact: sales@ ics-ltd.com RSC #1801 @ www.DSP-FPGA.com/catalogrsc

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ICS SENSOR PROCESSING

ICS-554

Designed for communications, radar, and test and measurement applications, the ICS-554 PMC module combines the best in ADC and DSP technologies to provide the ultimate advantage in cost, size, and performance. The ICS-554 includes four 14-bit ADCs sampling synchronously at frequencies up to 105 MHz. It includes four Graychip GC4016 quad digital downconverters for simultaneous downconversion of up to 16 arbitrary signal bands. Following the tuners, a 1 or 3 M gate Xilinx FPGA provides a powerful capability for baseband processing. It offers onboard storage and a fast PCI 2.2 64-bit, 66 MHz DMA interface.

FEATURES:

- Available in one-, two-, or four-channel versions with or without DDCs
- Up to 105 MHz simultaneous sampling of all channels
- Internal or external clock and trigger
- > 72 dB signal-to-noise ratio and > 85 dB spurious free dynamic range
- 1 MB onboard memory storage
- User programmable 3 M gate Xilinx FPGA with an uncommitted Pn4 user I/O PMC interface

For more information, contact: sales@ ics-ltd.com RSC #1802 @ www.DSP-FPGA.com/catalogrsc

Traquair Data Systems, Inc.

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Signalware ORS-1xx A/D/A Boards

The Signalware ORS-1xx boards offer a range of 12, 14, and 16-bit A/D/A, digital I/O, and FPGA capabilities as a peripheral with micro-line embedded DSP boards, daughter cards for TI DSKs, or as standalone devices.

An onboard Xilinx Spartan-IIE or Virtex-II FPGA adds flexibility to the ORS-1xx, enabling configurable interfacing options to micro-line-based DSP and FPGA resources, as well as an optionally user-programmable platform for implementing front-end data processing algorithms such as down-conversion or decimation. FPGA programming requires the use of an optional ORS-1xx FPGA programming package.

The FPGA interfaces to the micro-line connectors. It supports either a 32-bit data bus to a micro-line DSP EMIF or dedicated 16-bit data port for connecting with the Virtex-II FPGA of a micro-line C6713Compact (also listed in this publication).

The ORS-1xx may also be mounted on TI DSP Starter Kits (DSKs) using an ORS-900 adaptor card. This provides a convenient and low-cost way to build prototypes for full custom hardware solutions.

FEATURES:

- ORS-112
  - Four Analog Devices AD9260 ADCs offering 2.5 to 20 MSps depending on mode
  - Two TI DAC8532 16-bit DACs with two channels per DAC offering up to 625 kSps per channel
  - 12-bit or 16-bit mode A/D operation
- ORS-114
  - Two (four) Analog Devices AD9248 14-bit ADCs offering up to 65 (40) MSps per ADC- Two (four) Analog Devices AD9767 14-bit DACs offering up to 125 (40) MSps per DAC
- ORS-116
  - Two TI ADS8364 16-bit ADCs with six differential input channels per ADC offering up to 250 kSps per channel
  - Three TI DAC8534 16-bit DACs with four independent output channels per DAC offering up to 250 kSps per channel
- ORS-119
  - 6x 8-bit digital I/O
  - LVTTL: Up to 100 MHz switching rates
  - LVDSL: Up to 200 MHz switching rates
  - Opto-isolation also optionally available

For more information, contact: sales@ traquair.com

RSC #1901 @ www.DSP-FPGA.com/catalogrsc

Traquair Data Systems, Inc.

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Ultra-compact

Ultra-compact multi-chip modules provide TMS320C5000 DSP, Spartan-II, or Spartan-3 FPGA, and ready-to-use IEEE 1394a FireWire communication capabilities in a tiny 30 mm x 36 mm surface-mount PLCC package.

Ultra-compact modules are suitable for user-programmable DSP/FPGA resources or as FireWire connectivity devices. DSP and FPGA programming is optional and is not required for enabling FireWire.

The ready-to-use FireWire interface can be used for integrating digital cameras, sensors, and other embedded devices within a high-performance FireWire network. Data streaming across FireWire is supported at up to 32 MBps (sustained).

FEATURES:

- Texas Instruments TMS320C5000 DSP
- Xilinx Spartan-II or Spartan-3 FPGA
- Ready-to-use IEEE 1394a FireWire
- Up to 8 MB of SDRAM and 512 KB of Flash ROM
- RS-232, McBSP, I2C, JTAG, analog and digital I/O
- 116-pin, 30 mm x 36 mm surface-mount PLCC package

For more information, contact: sales@traquair.com RSC #2001 @ www.DSP-FPGA.com/catalogrsc

Blackhawk

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Mount Laurel, NJ 08054
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Your Source for Embedded Signal Processing

Blackhawk
Powering DSP Development™

LAN560 Emulator

The LAN560 JTAG Emulator (LAN560) from Blackhawk is the first of its class for debugging TI DSPs across Ethernet networks. The LAN560 supports all of the advanced capabilities of Texas Instruments' latest DSPs. These capabilities include high-speed Real-Time Data Exchange (RTDX)™ for lightning speed downloads, and advanced event triggering to quickly find and fix real-time software problems. Connections are made through its auto-sensing 10/100Base-T RJ-45 connector that attaches directly to any hub, switch, or wireless access point on the network. Blackhawk JTAG Emulators are available from a worldwide network of industry resellers.

FEATURES:

- 10/100Base-T Ethernet LAN interface with an internal TCP/IP stack enables direct connection of the LAN560 to the network
- High-speed RTDX™ support with data rates of more than 2 MBps and real-time, non-intrusive advanced event triggering capability
- New compact pod with power and link activity indicator; LEDs show operational status
- Standard high-speed USB 2.0 (480 Mbps) port is Windows® plug-n-play compatible, allowing an additional interface option

For more information, contact: sales@ blackhawk-dsp.com RSC #2002 @ www.DSP-FPGA.com/catalogrsc

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Mount Laurel, NJ 08054
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USB510 Emulator

The credit card-sized Blackhawk™ USB510 JTAG Emulator is the most compact and lightweight JTAG emulator available for Texas Instruments' TMS320, TMS470 (ARM), and OMAP families. The USB bus powered design, which requires no external power source, is the ultimate in portability resulting in an ultra compact unit that is very affordable. Blackhawk is the first company to introduce a USB JTAG emulator for Texas Instruments' DSPs, and the new USB510 sets the standard for portability, reliability, and ease of installation. Blackhawk JTAG Emulators are available from a worldwide network of industry resellers.

FEATURES:

- Ultra compact designed pod with status LED requires no external power and is powered completely from the PC's USB port
- Highly flexible micro-coax JTAG cable is designed to let users position the emulator and target debug hardware effortlessly
- Legacy support for Code Composer v4.1x and CCStudio v1.2 gives users access and compatibility to VC33, C20x, and C24x
- Standard high-speed USB 2.0 (480 Mbps) compliant port and Windows® plug-n-play installation

For more information, contact: sales@blackhawk-dsp.com RSC #2101 @ www.DSP-FPGA.com/catalogrsc

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PMC571

The PMC571 is the world's first rugged PMC to offer wide bandwidth ADC and DAC conversion capabilities for software radio applications. Combining it with Radstone's market-leading PowerPC and DSP capabilities will enable customers to create multifunction blade products offering ADC and DAC conversion, FPGA, DSP, and processing in a single-slot configuration.

A powerful 4 M gate FPGA provides the platform for application-specific software development within a Xilinx Virtex II environment. The 64-bit, 66 MHz PCI interface ensures compatibility with the latest generation Radstone Quad PowerPC, VMEbus, and CompactPCI boards.

FEATURES:

- 4 M gate FPGA, providing the platform for application-specific software development within a Xilinx Virtex II environment
- Sample rates up to 80 MHz and processing bandwidth of 40 MHz
- Full 64-bit, 66 MHz PCI interface and a 64-bit general-purpose I/O with 14-bit data conversion on ADC and DAC functions
- Air- and conduction-cooled ruggedization levels and extensive application and technical support data available
- Full source-code device drivers available for VxWorks and Linux

For more information, contact: sales@ ics-ltd.com RSC #2102 @ www.DSP-FPGA.com/catalogrsc

VMETRO Inc.

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Tel: 281-584-0728 • Fax: 281-584-9034
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Your Source for Embedded Signal Processing

VMETRO
innovation deployed

Vanguard PMC

Vanguard PMC bus analyzers debug, test, and validate in a PMC environment. This analyzer captures and displays up to 2 MS of bus activity at rates up to 133 MHz using powerful trigger and store qualifiers, and offers extensive system performance measurements. The exerciser emulates master or target devices and offers a script engine. The protocol checker detects 45 PCI and 71 PCI-X protocol errors. The analyzers are controlled via Ethernet or USB from a PC running Windows and VMETRO's BusView graphical user interface. The Ethernet port enables connection to Vanguard analyzers anywhere that a network connection is available.

FEATURES:

- 0-100 MHz PCI-X and 0-67 MHz PCI for PMC systems; 3.3 V and 5 V support
- 2 MS trace buffer at 256 bits
- Networked bus analyzer (built-in Ethernet port)
- Concurrent and independent operation of the analyzer, statistics, exerciser, and protocol checker functions
- Trace collapse/expand
- Compliance checker

For more information, contact: info@vmetro.com RSC #2201 @ www.DSP-FPGA.com/catalogrsc

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Spectrum Digital TI DSP Target Platforms

Processor Family	Target Module	Scan/Interface	Part Number	Price
TMS320C3x	D.Module.C31eco	MPSD	Call	Call
	MK31Vplus	MPSD	Call	Call
	MK32	MPSD	Call	Call
TMS320VC33	eZdsp™ VC33	PP/JTAG	701385	$ 519.00
	D.Module.VC33	JTAG	Call	Call
TMS320F24x™	EVM320F240	JTAG	701005	$ 795.00
	EVM320F243	JTAG	701015	$ 795.00
	EVM320LF2407A	JTAG	701019A	$ 795.00
	eZdsp™ LF2401A	PP/JTAG	761120A	$ 515.00
	eZdsp™ LF2407A	PP/JTAG	761119	$ 319.00
TMS320F28xx™	eZdsp™ LF2808/socket	USB/JTAG	761132	$ 469.00
	eZdsp™ LF2812	PP/JTAG	761128	$ 325.00
	eZdsp™ LF2812/socket	PP/JTAG	761129	$ 469.00
	eZdsp™ R2812	USB/JTAG	761130	$ 469.00
TMS320VC54x™	EVM320C548	JTAG	701070	$ 795.00
	EVM320VC549	JTAG	701072	$ 995.00
	EVM320VC5402	JTAG	701170	$ 895.00
	EVM320VC5406	JTAG	701190	$ 895.00
	EVM320VC5409	JTAG	701175	$ 995.00
	EVM320VC5410	JTAG	701173	$ 995.00
	EVM320VC5416	JTAG	701176	$ 1099.00
	Shruthi VC5416	JTAG	701821	$ 995.00
	DSK VC5416	USB/JTAG	701840	$ 415.00
	EVM320C54V90	RS232/JTAG	701191	$ 495.00
	EVM320C54CST	RS232/JTAG	701192	$ 495.00
TMS320VC55x™	EVM320DA255	JTAG	701852	$ 849.00
	EVM320VC5502	JTAG	701860	$ 995.00
	EVM320VC5509A	USB/JTAG	701857	$ 1495.00
	DSK VC5510	USB/JTAG	701880	$ 415.00
TMS320C6000™	D.Module.C6201	JTAG	Call	Call
	D.Module.C6203	JTAG	Call	Call
	D.Module.C6701	JTAG	Call	Call
	D.Module.C6713	JTAG	Call	Call
	DSK C6713	USB/JTAG	701895	$ 415.00
TMS320C64x™	DSK C6416T, 1Ghz.	USB/JTAG	701891	$ 515.00
	EVM DM642, 720 Mhz.	JTAG	702002	$ 1999.00
OMAP™	OMAP5912 OSK	JTAG	701875	$ 315.00
TMS470 ARM	EVM470	JTAG	701080	$ 1295.00

C6416T DSP Starter Kit

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FPGA or DSP for military applications? Both have their place

By Peter Cavill, President, Radstone Embedded Computing

In the military COTS marketplace, the number of technologies and standards vying for the customer dollar is certainly no less than in any other marketplace. VME or CompactPCI? StarFabric or InfiniBand? Freescale or Intel? In an ideal world of unlimited resources, every manufacturer would support all standards and implement all technologies. But, it's not an ideal world.

Superficially, a similar choice presents itself in the arena of signal processing. Is DSP technology the best solution, or does FPGA offer more? And are these the only two horses in the race?

The answer, of course, is that neither is "better," and there are other horses. Whether DSP or FPGA technology or any other design approach is "better" depends entirely on the characteristics of the application. Both have their place. In an industry that's as susceptible to becoming a victim of "bright shiny object" syndrome as any other – much recent media coverage seems to indicate that FPGAs are leaving DSPs trailing in their dust – that's a truth that can be easily forgotten. This article will try to redress the balance.

It is certainly true that the FPGA, now highly attractive to systems designers who previously would have only considered using DSP technology, has made substantial improvements in price and performance throughout the past few years. Although FPGA implementations are now widespread in a range of military and defense signal processing applications such as sonar, radar, image processing, and Software-Defined Radio, the DSP continues to find favor. Why is that?

First, it should be noted that digital signal processing is not a single application, but rather a complex inter-relationship between a number of applications, which can be broadly characterized as *front end* and *back end.* The developer's skill encompasses the ability to choose the right horse for the course using the criteria they have always used, which would typically include not only performance, but also power consumption, cost, time to market, memory usage, and programming requirements, among others.

The developer might start, for example, by considering whether the needed DSP functionalities could be implemented using an FPGA. Floating-point operations, for example, do not lend themselves well to an FPGA, and if accuracy is a key application requirement, then floating points will generally deliver at a higher degree. Applications such as SIGINT and ELINT that require large FFTs – for example, a million points or more – typically require floating-point operations, as fixed-point arithmetic will limit a dynamic range.

Similarly, processing involving matrix inversion (or division) is better suited to a DSP or General-Purpose Processor (GPP) platform. As an example, a typical beamforming or smart antenna system multiplies the received samples from multiple antennae with weights. While an FPGA is ideally suited to perform the very high-speed multiplications, dynamic computation of the weights requires matrix inversion, and is thus better suited for implementation using a GPP or dedicated DSP.

It is perhaps appropriate, at this point, to outline some of the fundamental differences between DSPs, GPPs, and FPGAs. DSPs, for example, operate at very high rates, but are limited to performing only a few operations at a time. FPGAs, on the

	DSP/GPP	FPGA
Programmability	Better	Worse
Parallelism	Worse	Better
Development time	Better	Worse
Available skills	Better	Worse
Power consumption	Better	Worse
Performance:		
Floating point	Better	Worse
Fixed point	Worse	Better

Table 1

other hand, typically operate at slower speeds than DSPs and GPPs but allow an almost unlimited number of operations to occur simultaneously (parallelism). Similarly, DSPs and GPPs tend to have excellent floating-point units for increased accuracy/dynamic range and are thus better suited to complex floating-point algorithms for decision-making. FPGAs are much better at fixed-point operations and parallelism, and are therefore better suited to tight, fixed-point mathematical operation such as filtering, which might occur at the front end of a signal processing solution.

The foregoing may appear to be trying to make a case in favor of DSP, pointing out possible reasons why it might be preferred over FPGA. The intent, though, is to reestablish a balance. Despite much of what is written, FPGA is not the answer to every developer's prayer, but for some applications, it unquestionably provides the most appropriate approach. Table 1 outlines where each technology's strengths lie, with the caveat, of course, that it is inevitably a subjective view. The specific application determines whether one is superior to the other.

FPGAs, for example, are extremely useful as front-end coprocessors used in conjunction with back-end DSPs or GPPs. As noted earlier, very high-speed filtering and beamforming applications can be effectively performed in an FPGA. Thus, having an FPGA colocated with data acquisition functionality greatly simplifies system architecture. Additionally, this usually reduces back-end data rate and, thus, processing load. As a result, a majority of ICS (part of Radstone Embedded Computing) software radio boards are fitted with a user FPGA suitable for application development. This configurable functionality makes the products attractive for a variety of applications and differentiates them from *just data acquisition and conversion* boards. The configurable user FPGA enables users to add functionality to the board, making system integration extremely straightforward. The data rate reduction that often occurs in these custom applications enables simplified software architecture and is useful in legacy processing modules for a phased upgrade of system functionality.

In fact, any discussion of signal processing technology would be incomplete if it did not also include discussion of the role of the GPPs. In the same way as FPGA technology is appropriate for some applications and DSP technology for others, so, too, there are applications where a GPP approach is preferable.

Take, for example, the PowerPC/AltiVec combination at the heart of Radstone's G4DSP family of DSP boards. It's an attractive architecture to many customers for a number of reasons. In appropriate applications, it's certainly capable of outperforming a solution based on FPGA or *traditional* DSP technology, but that's only part of the story. Perhaps just as importantly, it leverages the broad industry infrastructure of experience and expertise in C and C++ programming. Beyond that, the maturity of AltiVec technology means that there is widespread operating system support for it, together with a highly developed and stable set of supporting tools. Choosing the GPP approach rather than a DSP or FPGA may result in a shorter development cycle and faster time to market.

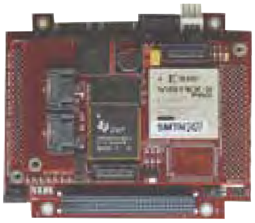
In addition, for applications such as front-end wideband digital down conversion, for example, where FPGA performance is highly desirable, the opportunity exists to combine the capabilities of the G4DSP with ICS ADC and DAC PMCs to create an extraordinarily powerful, single-slot blade, DSP solution.

In summary, FPGAs, DSPs, and GPPs have their place – a place determined by the application and customer needs. Therefore, a coexistence, rather than a competition, emerges as the obvious way forward. Each technology has its advantages and disadvantages, and each is capable, according to the application, of outperforming the other. At Radstone, we know we don't have to choose which technology to support since our customers expect us to support the technology that is right for their needs.

For more information, visit the Radstone website at www.radstone.com.

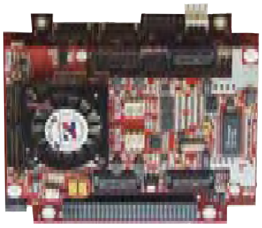
SUNDANCE

SMT287
PC/104 Disk Storage Solution



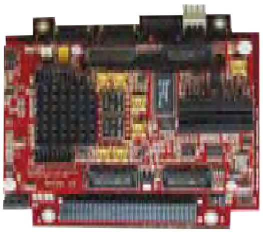
This is an example unit made up of SMT130 carrier and SMT387 module with 'C6415 DSP; Virtex II VP20; SATA Link; and Rocket Serial Link (RSL). In this solution the DSP can directly write to or read from Serial ATA hard disk supporting FAT32 filing system.

SMT290-VP7-5
PC/104 two channel ADC



An ADC Module with 2-Channels of each, sampling at 210MSPS @ 12bits. This is the first DAQ module to use a Virtex-II Pro FPGA and a unique 'Double-Decker' inter-connections concept that separate the Digital control functions from the noise-sensitive DAQ semiconductors.

SMT291
PC/104 two channel ADC



Built on the SMT391 module this combination provides a two channel ADC sampling at 1GHz per channel with 8bits resolution.

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Quixote

Quixote is a 64-bit CompactPCI 6U board for advanced signal capture, generation, and coprocessing. It combines one C6416 DSP with a two- or six- million-gate Virtex-II FPGA, utilizing the best of both worlds in signal processing technology to provide extreme processing flexibility and efficiency and deliver unmatched performance. Dual 105 MHz analog inputs/outputs integrate signal capture and waveform generation right on the FPGA external interface. One PMC site facilitates integration of off-the-shelf or custom PMC mezzanine boards. PCI-to-StarFabric bridge offers two 2.5 Gbps ports to the new PICMG 2.17 switched interconnect backplane.

FEATURES:

- 1 GHz TMS320C6416 DSP
- 2-6 MGATE Virtex-II FPGA
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- AD6645 & AD9764 converters
- 64/32-bit CompactPCI, 66 MHz, 5 V/3.3 V
- Complex trigger modes with HW event logging

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Quadia is a quad-DSP, dual FPGA, dual PMC site, CompactPCI board with an advanced architecture that provides the best interprocessor connectivity and access to the finest external interfaces available today, to deliver blazing performance and extreme flexibility for advanced signal capture and real-time processing applications. The board features four C6416 DSPs split in two independent clusters, each hosting a PMC site and one large FPGA for end-user code, a central FPGA routing interprocessor communication, end-user FPGA communication, external port serial I/O for PCI-Express or other private link, global memory, and PCI interface.

FEATURES:

- 720 MHz TMS320C6416 DSP (x4)
- 64 MB SDRAM per processor
- Flexible internal/external communication mesh
- 64-bit/66 MHz CompactPCI
- Two PMC sites with Jn4 to FPGA
- External data port, up to 12 Gbps

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Danville's SHARC-based dspstak and dspblok families simplify DSP-based embedded applications using the latest Analog Devices SHARC DSPs.

Each dspstak consists of a DSP engine and one or more I/O modules. A dspstak DSP engine consists of a SHARC, Flash and EE memory, programmable clocks, and RS-232 and USB interfaces. There are dspstak boards that include an Analog Devices onboard debugger (ICE). These boards emulate an Analog Devices EZ-KIT and, at the same time, create production-ready, off-the-shelf solutions.

Danville's dspblok DSP modules are small plug-ins (60 mm x 60 mm) that allow DSP functionality to be easily added to your product.

FEATURES:

- Analog Devices ADSP-2126x and ADSP-2136x SHARC DSPs
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- Code examples and libraries for easy software development
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- Separate I/O modules allow flexible configurations

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micro-line C6713CPU

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The C6713CPU can function as a standalone system or as a mezzanine daughter card embedded within a larger system or design. Optional data acquisition modules are available. Developers can easily integrate their own hardware with the DSP or FPGA.

FEATURES:

- Texas Instruments TMS320C6713 DSP
- 64 MB of SDRAM (128 MB SDRAM available on request), 2 MB Flash ROM
- Optionally programmable Spartan-3 FPGA (up to 1 M gate density)
- RS-232 interface (up to 691.2 kBaud), onboard temperature sensor
- Space saving 98 mm x 67 mm board size
- CE certified, ISO9001:2000 accredited production

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micro-line C6713Compact

The micro-line C6713Compact offers a highly flexible DSP/FPGA single-board solution for developers requiring integrated DSP, FPGA, and FireWire resources. It can function as a standalone system or as a mezzanine daughter card embedded within a larger system or board design. The C6713Compact incorporates a high-performance TMS320C6713 floating-point DSP together with onboard Virtex-II FPGA and IEEE 1394a FireWire communications interface resources. For situations that require additional functionality, developers can extend the capabilities of the C6713Compact using optional data acquisition and I/O modules or their own application-specific hardware. External hardware can interface easily with the TMS320C6713 processor or connect directly to the Virtex-II FPGA.

Optional analog interfaces: Analog interfaces supporting multichannel 12-bit, 14-bit, and 16-bit A/D/A are optionally available. I/O data can transfer across the DSP EMIF or can optionally stream through the Virtex-II FPGA to reduce DSP load (for high bandwidth applications).

Embedded data storage: Mass storage with FAT32 support is available with the optional Embedded Storage API when used together with FireWire-enabled hard drives or CompactFlash devices.

Networking and connectivity: The onboard FireWire interface facilitates C6713Compact integration with other embedded DSP resources, cameras, sensors, and host computers. FireWire provides guaranteed bandwidth for mission critical applications, live connect/disconnect, and many other impressive features. 10/100Base-T Ethernet communications can be added using the SC100Base-Tx daughter card and the Windmill Innovations eXpressDSP-compliant bf3Net TCP/IP protocol stack, and embedded Web server software.

Imaging and frame capture capabilities: Imaging and frame capture configurations are easily realized with optional software support for IIDC IEEE 1394a FireWire digital cameras.

FEATURES:

- Standalone and embeddable DSP/FPGA board
- Texas Instruments TMS320C6713 floating point DSP
- 250 k, 500 k, or 1 M-gate complexity Virtex-II FPGA
- 400 Mbps IEEE 1394a FireWire interface
- 32 or 64 MB of 100 MHz SDRAM and 8 MB Flash EPROM
- Optional 12-bit, 14-bit, and 16-bit multichannel analog I/O support
- Optional 10/100Base-T Ethernet, TCP/IP, and Web server support
- Optional support for hard drive and CompactFlash embedded data storage
- Universal interfaces to connect to peripheral devices
- Board dimensions: 120 mm x 67 mm
- ISO9001:2000 accredited production and CE certification

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micro-line C6x11CPU

The micro-line family of embedded DSP boards provides a range of TMS320C6000 DSPs for commercial and industrial applications. Developers can use them as standalone embedded DSP systems, or as integrated mezzanine plug-in modules with customer/application specific hardware designs.

The micro-line C6x11CPU DSP board combines either a fixed point TMS320C6211 or a floating point TMS320C6711 DSP with SBRAM, SDRAM, Flash ROM, and the micro-line bus interface.

The C6x11CPU is easily integrated into larger system designs. Options are available for FireWire and Ethernet connectivity, as well as analog and digital I/O.

FEATURES:

- Texas Instruments TMS320C6211 or TMS320C6711 DSP
- Up to 2 MB of SDRAM or up to 64 MB of SDRAM
- Up to 512 KB Flash EPROM, McBSP, and RS-232
- Optional FireWire, Ethernet, analog and digital I/O
- Space saving 98 mm x 67 mm board size
- CE certified, ISO9001:2000 accredited production

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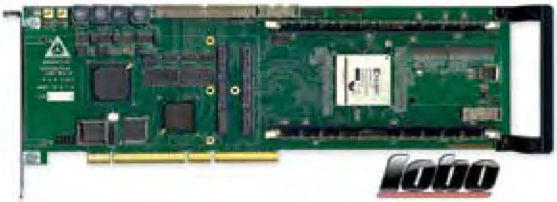

FEATURES:

- 225 MHz/1350 MFLOPS TMS320C6713 DSP
- 3 or 6 M gate Virtex-II FPGA
- 32 MB SDRAM, Up to 2 GB DDR SBSRAM for FPGA
- Separate receive/transmit channels
- External I/O interface for data card with two 80-pin connectors to FPGA DIO for 2+ GBps rates

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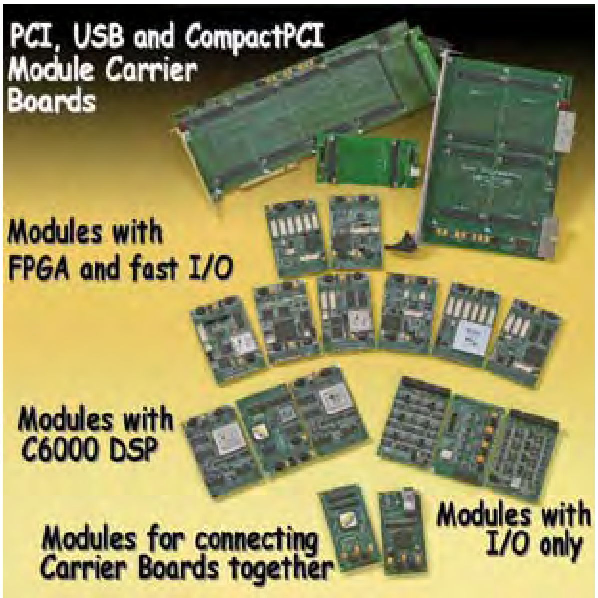
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- Interboard connection modules available for larger or distributed systems
- System development tools, IP, software demos, examples, and tutorials included
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MIRAGE-NP2 is a next-generation, dual-channel, universal JTAG/MPSD emulator for all TI TMS320 DSP platforms designed for mobile, desktop, and industrial host PCs with a PCMCIA PC card (CardBus) slot. The MIRAGE-NP2 has the industry's longest 2 m (6.6 ft) connection cable, universal JTAG/MPSD pod (UniPod), target 0.5 V to 5 V power voltage support, programmable 0.5 MHz to 30 MHz JTAG clock, fast TAG/MPSD upload/download speed and RTDX, embedded target diagnostic, ultra compact and ultra light-weight design, as well as simple Plug-and-Play installation. All of these features in one package make MIRAGE-NP2 an ultimate "all-in-one" emulation and diagnostic tool and "must have" instrument for all DSP hardware and software engineers for both mobile and desktop workstations. Maintaining a leadership in the industry, the MIRAGE NP2 is the first to integrate a universal JTAG/MPSD emulator with target diagnostic features such as target power voltage measurement and path clock frequency. It is the first to introduce a universal, ultra compact and ultra light-weight JTAG/MPSD UniPod, thus saving the user effort and time, and providing extraordinary comfort in debugging all user DSP devices.

FEATURES:

- Supports all TI TMS320 DSP platforms, including: C2xxx/C5xxx/C6xxx, OMAP, ARM, C30/C31/C32/VC33, C4x, C5x, and more
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- LED indicators at UniPod for target status; high noise immunity; faster than LPT port and USB emulators; supports target JTAG and TI MPSD ('C3x) scan paths
- Available with one (MIRAGE-NP2/1)and two-(MIRAGE-NP2) emulator channels installed
- Plug-and-Play installation in notebook, desktop, or industrial PCs with a PCMCIA Type II PC card (CardBus) slot;
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PMP1000

Performance

Signatec harnessed the power of nine Texas Instruments C6414 DSPs to offer the perfect solution for all demanding processing applications. Signatec's PMP1000 delivers 72 GIPS of processing power with enough bandwidth to enable 1 GBps of processing throughput. Bottlenecks are reduced by the 2.6 GBps of concurrent onboard I/O.

Ease of programming

Beyond its awesome processing power, the PMP1000 software development system and onboard real-time OS make parallel processor programming easier than ever before. Signatec's software includes a development environment that seamlessly connects development tools from Signatec, the PMP1000's OS, Texas Instruments and Microsoft Visual C into a user-friendly environment running under Windows 2000/XP. This feature makes the PMP1000 very easy to use for the fast delivery of solutions.

Connectability

With three data communication interfaces to the outside world, the PMP1000 is an essential component of a completely integrated system. Connect Signatec's high-speed waveform recording boards through the Signatec Auxiliary Bus (SAB), combined with the PMP1000's PCI-X interface, and users are empowered to acquire, transfer, process, and store real-time data simultaneously with no breaks in the analog record for data rates up to 1 GBps.

The ability to connect the PMP1000 to any number of customer-specific channels of data for exceptionally high continuous data throughput rates makes it the most flexible solution for advanced radar, signal intelligence (SIGINT), data fusion, software defined radio, and high-speed ultrasound applications.

Custom feature for optimized solutions

The PMP1000's third bus interface will enable high-speed external connections to an interchangeable "piggy-back" module, delivering up to 1 GBps of data throughput. The external interface module makes the PMP1000 highly customizable, allowing users to connect this board to any desired data source.

FEATURES:

- 72 GIPS of processing power
- Parallel ppocessing with up to 9 TI C6414 DSPs
- 2600 MBps internal I/O via switching network
- 64 MB of addressable memory mapped into each of the eight main processing DSPs (> 512 MB of total DSP memory)
- Unique program execution processor for dynamic thread allocation
- Advanced parallel DSP OS simplifies user programming
- Customizable external interface for accommodating any type of user data channels
- 2.5 GBps of total external I/O via three interfaces
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- 1.3 GBps peak transfer into DSP memory
- Enhanced OS scheduler built on TI's DSP BIOS technology
- Designed to create true high-speed, real-time systems in otherwise non-real-time environments, such as the PC

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VT-4000 FPOA Board

The VT-4000 Reconfigurable Processor provides a new approach that offers significant performance advantages. Based on MathStar's Field Programmable Object Array (FPOA) technology, the VT-4000 delivers high performance reconfigurable functionality with flexable I/O on an industry standard platform. Combined with powerful high-level software tools, the VT-4000 provides an advanced rapid-prototyping environment for developing solutions to demanding signal processing applications.

The VT-4000 architecture incorporates the MathStar SOA13D40 Field Programmable Object Array (FPOA). The FPOA is a reconfigurable array with hundreds of configurable processing elements with 1 GHz internal clock speed, internal register files and block RAM, external DDR memory controllers, and flexible high-bandwidth I/O interconnect. Two banks of RLDRAM II external memory are provided for FPOA, organized as 16 M x 36 bits per bank.

One of the FPOA GPIO ports is connected to an onboard PCI bridge to facilitate host computer access to the FPOA internal data and control paths, internal block RAM, and and external DRAM. The remaining three GPIO ports and LVDS port are connected to a mezzanine module interface to provide modular I/O capability. The FPOA can be configured directly using a front panel accessible JTAG port, or a configuration ROM can be programmed and the FPOA configuration will automatically be loaded on system power up. A complete set of development tools are available for the VT-4000.

The VT-4000 is the ideal development system for demanding applications where "ASIC-like" performance is required on an "FPGA-like" development schedule. DSP applications include advanced imaging pattern recognition, synthetic aperture radar, signal intelligence, wireless communications, and Software Defined Radio.

Valley Technologies' VT-4000 is the world's first Field Programmable Object Array-based reconfigurable computing module.

FEATURES:

- The VT-4000 is the world's first Field Programmable Object Array (FPOA) board with internal FPOA clock speeds to 1 GHz
- The VT-4000 FPOA development board yields ASIC-like performance at COTS prices
- 100 MHz LVCMOS GPIO, 3 x 44-bit, with 12-bit control 128 MB, 250 MHz DDR RLDRAM II
- 16-bit Rx/Tx, 800 MHz DDR LVDS I/O with programmable deskew is provided
- The VT-4000 provides JTAG or EEPROM configuration; remote reconfiguration of the VT-4000 is easy
- PCI local bus bridge with universal signaling 32-bit/66 MHz DDR LVDS I/O is provided
- The VT-4000 is currently available in a 6 U x 160 mm CompactPCI format; other configurations can be provided
- Mezzanine module interface for modular I/O capability is standard on the VT-4000
- A complete set of development tools are available, including the Valley Technologies "MAGI" Development/Deployment Environment
- VTI's VT-4000 board is supported by a complete and fully integrated hardware and software development platform
- VTI's application department is capable of supporting new applications from specification through prototype and delivery
- An Internet demonstration of the VT-4000 FPOA-based development system can be arranged by calling Valley Technologies, Inc.

For more information, contact: bob@ valleytech.com

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FPGAs rise to meet increasing DSP system requirements

By Brian Jentz, Senior Product Marketing Manager, Altera

DSP technology is quickly becoming a driving force within the semiconductor industry as the result of the growing architectural complexity of DSP systems. Computational performance requirements for these systems have outstripped what standalone DSP functions can provide. Rather than using design alternatives such as Application-Specific Integrated Circuits (ASICs) or Application-Specific Standard Products (ASSPs), designers are increasingly turning to FPGAs for a flexible and more cost-effective solution, enabling them to get their products to market as fast as possible.

In the video market, the transition from standard-definition MPEG2 to high-definition H.264 represents an increase in architectural complexity of 20x. In wireless, the transition from 16-channel 2G boards to 128-channel 3G boards has resulted in an even greater increase in this complexity over the last several years. At the same time, FPGAs have evolved to better support DSP applications, offering the flexibility to implement custom interfaces and peripherals and the capability to scale algorithm complexity and channels as feature requirements grow and change. Providing more than 180,000 Logic Elements (LEs) and 384 18 x 18 multipliers, today's FPGAs are capable of handling algorithms once thought to be the exclusive domain of ASICs and ASSPs. For example, system developers are implementing standard-definition, main profile H.264 encoders in a single FPGA, a capability that would have consumed several FPGAs in previous generations. Implementation in an FPGA rather than an ASIC or ASSP means at least a six-month gain in time to market. High definition, main profile H.264 encoders still require multiple FPGAs, but this is still the most effective solution with FPGAs being adopted widely for this purpose. The move from 130 nm to 90 nm has spurred a 10x increase in DSP performance in FPGAs. With this trend expected to continue, a single-chip H.264 high-definition encoder will likely be reality in 65 nm-based FPGAs.

An equally exciting trend is the amount of processing power that low-cost FPGAs deliver. In 1996, US $25 would buy about 1,000 LEs. Today, this amount (depending on the product) can buy 33,000 LEs, 500 Kb of RAM, and 35 embedded 18 x 18 multipliers. This performance and cost advantage makes FPGAs the ideal solution for DSP applications in such products as base stations, camcorders, security systems, televisions, and other video processing products. As FPGAs continue to integrate more memory and embedded functionality into complex systems, and as device costs continue to decrease, designers will be able to use them in an even wider range of DSP applications.

Flexible, fast, and low-cost path to market

Structured ASICs allow designers to migrate an FPGA design to a more efficient device once programmability is no longer needed. Structured ASICs cost roughly one-tenth the price as equivalent FPGAs; a typical design will run about twice as fast and consume about half as much power when implemented as a structured ASIC instead of an FPGA.

Engineers build structured ASICs by integrating logic and hard IP into standard base layers. Designers then customize the base array using the last few metal layers, offering faster development time combined with low unit cost. Altera provides the capability to directly convert an FPGA design into a pin-compatible structured ASIC, which thus offers designers a seamless path from FPGA to structured ASIC.

Optimized functionality

To improve time to market, system designers wanting to build DSP functionality into an FPGA also have a rich portfolio of highly optimized, customizable, off-the-shelf Intellectual Property, (IP) cores available. These cores include:

- FIR, FFT, JPEG2000, and H.264
- Interfaces for advanced memories, such as DDR2 and QDRII SDRAMs
- A wide range of peripherals, such as PCI, USB, and Ethernet

Powerful embedded RISC processors are also available. Using an off-the-shelf, pre-verified IP core frees the designer from reinventing the wheel at the functional design level, reducing both design time and cost. Since manufacturers have already optimized these cores for FPGA architectures, the designer can focus valuable development time on optimizing system-level features. The number of IP functions available to support DSP systems is increasing rapidly as more engineers target FPGAs for their algorithm development.

Several tools also exist to speed up DSP algorithm design in FPGAs. Synthesis tools from Altera, Synopsis, and Synplicity are able to infer the use of embedded DSP features, such as multipliers, from RTL code. The Mathworks provides a model-based design platform called Simulink. The combination of Simulink with Altera's DSP Builder or Synplicity's Synplify DSP enables system level simulation and hardware generation from the same environment, reducing algorithm development time. Several companies, including Celoxica and Impulse C, have targeted C-based design for FPGAs.

> "FPGAs are increasingly able to address the performance and features that DSP applications require today, all at a lower system cost."

Designers using such development tools and IP previously can integrate DSP algorithms with Altera's system tool, SOPC Builder. SOPC Builder eases design when a digital signal processor is used in conjunction with an FPGA. Using the SOPC Builder component editor feature, designers can easily interface to a DSP device. If a designer creates an SOPC Builder component interface to a processor, the designer can add additional I/O pins, pre-packaged peripherals, or custom, self-made peripherals in just a few mouse clicks. See Figure 1. SOPC Builder will build the system and output header files for the software development team. The team can access the peripherals from the external processor using their favorite Integrated Development Environment (IDE).

Unlike ASIC development tools, these design tools are typically available for a relatively low licensing fee. Third-party, C-based tools also support this design flow. Off-the-shelf DSP development kits, optimized for image and video processing systems as well as wireless applications, are available for design verification. Using such IP cores and automated-tool design flows, a system designer can decrease the design time by half for a particular function.

Complementary combination for a winning design solution

In today's market, with increasing competitive pressures and shorter product life cycles, designers have less time to develop and differentiate higher performance, more complex DSP designs. At the same time, FPGAs are increasingly able to address the performance and features that DSP applications require today, all at a lower system cost. As time-to-market and cost reduction pressures intensify, the combination of FPGAs and structured ASICs will give designers a risk-free, low-cost design solution that addresses a majority of DSP applications.

For more information, visit the Altera website at www.altera.com.

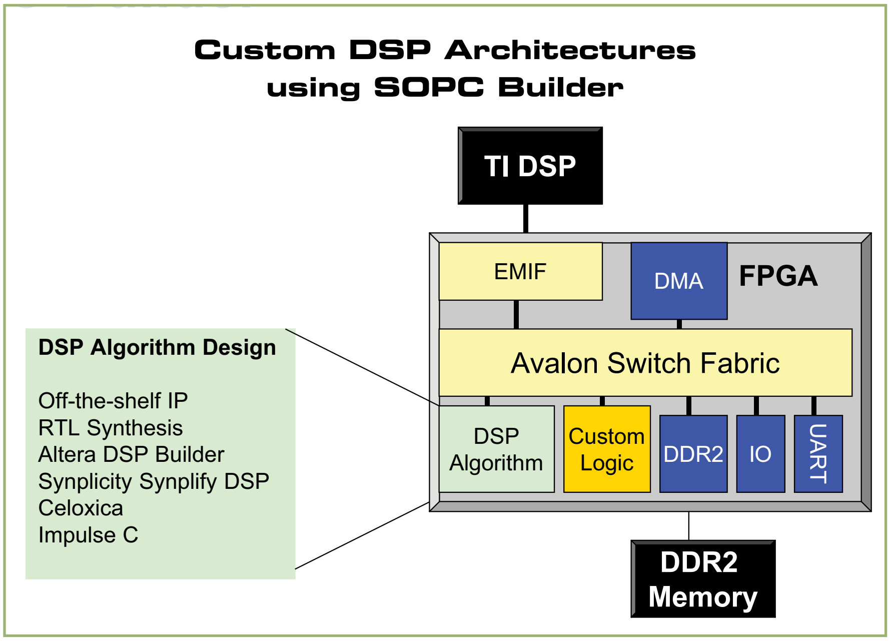
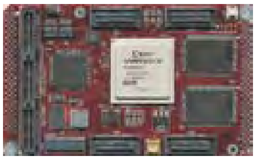


Figure 1

SUNDANCE

SMT368 SX35 virtex 4

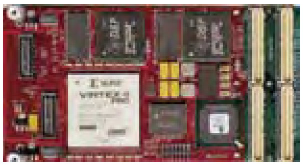


The Xilinx Virtex 4 SX has the highest amount of DSP blocks in the Virtex4 range, and the FPGA also has direct access to 8MBytes of ZBTRAM. The on-board PROM enables the module to be used 'Stand-Alone'. The three Sundance LVDS Bus (SLB) connectors with 36 pairs of Low Voltage Differential Signals can be interfaced over a long distance to some external control equipment, or act as an interface to an SLB mezzanine module like the SMT390 210MSPS ADC or the SMT391 1GHz ADC Module.

SMT395Q 4x1GHz TMS320C6416T

SMT395Q uses 4 TMS320C6416T DSPs, with a clock speed of 1GHz. It includes a Xilinx VirtexII-Pro VP70 FPGA, which provides 'C4x style Comm-ports, a TIM compatible enhanced global bus, two Sundance High-Speed Busses (SHBs), 14 Rocket IO serial links, and other control functions. Fully supported by TI CCS and the Diamond RTOS on PCI, CPCI and VME platforms.

SMT407 PMC 64bits 66MHz PCI interface



SMT407 includes 2 * TMS320C6416T DSPs at 1GHz each and a Xilinx VirtexII-Pro VP50. Interfaces include two Sundance High-Speed Busses (SHBs) and one FPDP interface through a programmable IO daughter module. 12 Sundance Rocket IO Serial Links (RSL), and other control functions are also available on the module. With the large Virtex-II Pro VP50 FPGA, pre-processing can be done on-the-fly before the DSP gets the data. SMT407 is supported by the TI CCS and 3L Diamond.

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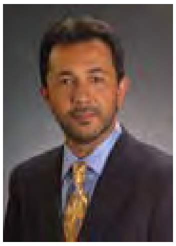
A TRULY SCALABLE SOLUTION

Reconfigurable DSPs – they're fast and flexible, but are they accessible?



By Omid Tahernia, VP & General Manager, DSP Division, Xilinx

Reconfigurable signal processing architectures hold great promise for creating high-performance DSP solutions. However, truly fulfilling that promise has proved elusive. In the past, proprietary reconfigurable DSP architectures have delivered on two essential criteria – performance and flexibility. Unfortunately, by failing to make these architectures broadly accessible from a robust suite of industry standard design tools, they never truly delivered the promise, often to the detriment of the companies that developed them.

On the other hand, some reconfigurable signal processors, such as FPGAs, continue to grow in popularity as ASIC replacements or high-performance coprocessors for DSPs.

FPGAs as reconfigurable signal processors

Through compelling features like 512 integrated DSP MACs that each deliver up to 500 MHz performance and consume as little as 29 µW/MHz of power, today's FPGA architectures are well suited for high-performance DSP applications because they provide a relatively straightforward path to highly parallel implementations of DSP functions. The efficient use of parallelism in DSP solutions can translate to orders-of-magnitude performance enhancements over traditional processor-based DSP architectures, which makes FPGAs ideal performance accelerators for conventional DSP processors (see Figure 1). Add to this the inherent ability to dynamically reconfigure an FPGA-based DSP solution, and it becomes readily apparent why the FPGA has grown in popularity as a high-value, low-risk DSP platform.

Accessibility for today's design teams

However compelling the FPGA's inherent performance and flexibility might support arguments for its use as a DSP platform, the one benefit that truly sets it apart as a reconfigurable processor is its accessibility – the ease with which designers with different backgrounds and skill sets can solve their particular DSP design problems. DSP system design involves the coordination of multiple design disciplines, including:

- System engineering
- Algorithm development
- Hardware design
- Software programming

As the mix of engineers, and hence the skill base, varies from company to company, the best way to accommodate each of these disciplines is to provide a design environment that allows each engineer to tackle their design problem in the language or tool best suited to their need.

The system designer provides the high-level definition and model of the system and, therefore, must make critical design decisions based on an analysis of the performance, size, and form factor requirements. This task requires a medium such as C or Simulink that provides rapid feedback and, therefore, rapid iteration/exploration of the design space.

The algorithm developer must be able to quickly evaluate different forms of the algorithms and explore the solution space to see which alternative is most able to meet system requirements. The majority of algorithm designers use MATLAB for its rich set of native constructs, easily available block sets, and good display cockpit. Until recently, the path from MATLAB to gates has been cumbersome and has involved much manual work. With the introduction of Accelchip, designers can now develop complex algorithms utilizing matrix multiplies or linear algebra and automatically generate RTL.

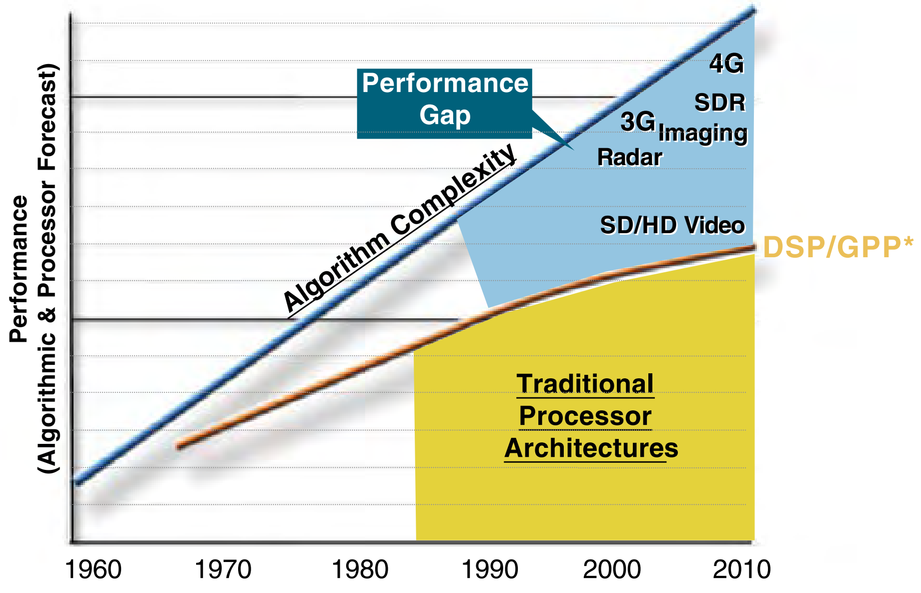
The role of the FPGA hardware designer today has expanded to include qualifying and verifying the IP blocks within the circuit, evaluating reuse of existing blocks, and developing new blocks based on requirements. These hardware designers usually work in hardware description languages such as VHDL and Verilog, and often have optimized legacy code that they need to be able to reuse.

The software developer is the team member most concerned with issues of coding DSPs and general-purpose processors. They most commonly use C and might also use assembly language to exploit additional performance.

Diversity demands development tool flexibility

With such diverse needs in today's typical design team, the ideal way to access the FPGA is to use a tool or framework that brings together multiple capabilities and abstractions, thereby enabling the designer to work in the problem language. Such a tool serves as a framework in which designers can interface the appropriate tools for each discipline – a sort of *plug-and-play* design environment such as System Generator for DSP available from Xilinx.

FPGAs Complement DSPs as
Algorithmic Complexity Outpaces Moore's Law



* Source: Jan Rabaey, BWRC

Figure 1

Providing a single environment that links vendor-specific design, implementation, and debug tools with widely used point tools for simulation, modeling, algorithm development, and synthesis, tools such as Simulink, ModelSim, MATLAB, AccelChip, Embedded Development Kit, Catapult C, Celoxica, Synplify Pro, and a host of others are the best way to ensure the broadest level of accessibility to the entire design team. Moreover, this plug-and-play design methodology allows designers to purchase only the tools needed for the problem at hand. In this fashion, design teams can use their preferred methodology based on the available team's skill set without paying for unnecessary capabilities.

In essence, the secret to enabling effective high-performance reconfigurable DSP system design is to offer design teams the ability to configure and reconfigure architectures to suit their ideal design algorithms with the accessibility to work in the most appropriate language for their particular discipline and skill set, and to use commercially available design tools. FPGA suppliers will need to rise to the challenge if they are to avoid the fate of other reconfigurable DSP counterparts.

For more information, visit the Xilinx website at www.xilinx.com.

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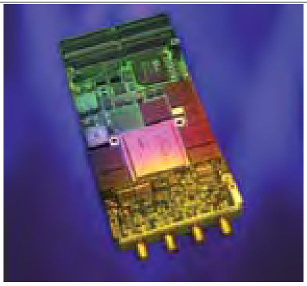
ADM-XRC-4



The ADM-XRC-4 series, FPGA-based PCI Mezzanine Card exploits the rich feature set of the latest Xilinx Virtex-4 devices. A comprehensive software development kit supports high-performance memory and I/O and host interfaces. The ADM-XRC-4 is the ideal COTS solution for prototyping and development all the way through to production.

Applications include radar and sonar processing, Software Defined Radio (SDR), reconfigurable computing, telecommunication encryption/compression, image processing, and Electronic Intelligence (ELINT).

FEATURES:

- FPGA: Xilinx Virtex-4 SX55 and LX60 to LX160
- SRAM: Four or six banks of 72 Mb ZBT
- Host interface: PMC, PCI, CompactPCI, and VME
- I/O: XRM adapters for SDRAM, LVDS, and analog
- Software: Win/Linux/VxWorks API and design templates

For more information, contact: info@ alpha-data.com RSC #3801 @ www.DSP-FPGA.com/catalogrsc

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ICS-1580

The ICS-1580 baseband processor is an FPGA-based PMC card, centered around the Xilinx Virtex II Pro. This powerful FPGA has been surrounded with resources to support the most demanding embedded processing applications. Onboard memory includes four banks of SDRAM, four banks of high-speed QDR II SRAM, and two 128 Mb Flash memory devices.

Despite the abundance of peripheral resources, a large portion of the Virtex II Pro has been reserved for end-user applications. ICS provides a complete HDK/EDK for the Xilinx ISE Foundation tool set, streamlining the development of new FPGA applications.

FEATURES:

- Xilinx Virtex II Pro FPGA with two on-chip PowerPC™ processors
- Linux kernel pre-installed
- 64 MB of SDRAM, 18 MB QDR II SRAM, and 64 MB Flash memory
- High-speed serial switched fabric I/O
- Window, Linux, and VxWorks software device drivers
- Extensive application and technical support available

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Cyclone II FPGAs & Dev. Kit

Altera® Cyclone™ II FPGAs are optimized for minimum die size and low cost, while offering the performance benefits of first-generation Cyclone devices, including a customer-defined feature set, industry-leading performance, and low power consumption. They also offer greatly increased density and more features, all at significantly lower cost. The Cyclone II family provides flexible hardware solutions that include up to 150 18-bit x 18-bit or 300 9-bit x 9-bit multipliers capable of implementing common DSP functions such as filtering, correlation, transforms, encryption and error correction, and video and image processing. Embedded multipliers provide more speed and logic efficiency compared to logic element (LE)-based multipliers. For more expandability, Cyclone II M4K memory blocks can implement high-performance soft multipliers for low-cost applications such as image processing, audio processing, and consumer electronics. The multipliers' data widths, coefficient widths, and precision can be customized for optimal DSP implementation.

The DSP Development Kit Cyclone II Edition delivers a complete turnkey DSP development environment for the entire design process from conception through hardware implementation, providing everything needed to leverage the industry-leading Cyclone II family in high-volume DSP applications. It includes a Cyclone II DSP development board, DSP Builder, Quartus® II development software, MATLAB/Simulink evaluation software, evaluation Intellectual Property (IP) cores, system reference designs and labs, and power supplies, cables, and documentation. This kit also offers an easy-to-use development platform that shortens DSP design cycles by helping designers create the hardware representation of a DSP design in an algorithm-friendly development environment. These tools reduce time to market, while making it easier for engineers to optimize design performance.

See www.altera.com/dsp for more information.

FEATURES:

- Industry's lowest-cost programmable logic platform for DSP implementation
- Offers up to 68,416 LEs of logic density and 1.1 Mb of embedded memory
- Delivers up to 150 18-bit x 18-bit embedded configurable multipliers operating at up to 250 MHz for low-cost DSP applications
- Supports an extensive IP portfolio and Nios® II processor implementations
- Facilitates FPGA coprocessor hardware acceleration implementations
- DSP development kit delivers a complete turnkey DSP development environment
  - DSP development board with a Cyclone II FPGA
  - Variety of analog and digital I/Os
  - 256 MB DDR2 DIMM, 1 MB synchronous SRAM, two EPCS64 devices
  - MATLAB/Simulink evaluation software, DSP Builder (one-year license), Quartus II DKE (one-year license)
  - Evaluation IP cores, system reference designs, and labs
  - Cables and accessories

For more information, contact: newsroom@ altera.com

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Stratix II FPGAs & Dev. Kit

Altera's 90-nm Stratix® II devices are the industry's biggest and fastest FPGAs, and feature an innovative logic structure that packs more functionality into less area, dramatically reducing device costs. With internal clock frequency rates up to 500 MHz and typical performance >250 MHz, these devices deliver on average 50 percent faster performance and more than 2 x the logic capacity than first-generation Stratix FPGAs. Stratix II FPGAs deliver 50 x higher multiplier bandwidth than single-chip, standalone DSPs. The DSP blocks have the flexibility and performance to implement fast, arithmetic-intensive applications such as image processing, wireless communications, military, broadcast, and medical. Each DSP block has dedicated multi-width multipliers, available in 36 x 36, 18 x 18, or 9 x 9 widths to implement DSP algorithms and functions, including filtering, video and image processing, correlation, transforms, encryption, and error correction. Stratix II FPGAs offer high DSP throughput to meet the requirements of emerging standards and protocols such as JPEG2000, MPEG-4, H.264, 802.16x, CDMA2000, 1xEV-DV, HSDPA, and W-CDMA.

The DSP Development Kits, Stratix II Edition, deliver a complete turnkey DSP development environment for the entire design process from conception through hardware implementation, providing everything needed to leverage the industry-leading Stratix II family in high-performance DSP applications. They include a Stratix II DSP development board, DSP Builder, Quartus® II software, MATLAB/Simulink evaluation software, evaluation IP cores, and system reference designs and labs. These kits also offer an easy-to-use development platform that shortens DSP design cycles by helping designers create the hardware representation of a DSP design in an algorithm-friendly development environment. These tools reduce time to market, while making it easier to optimize design performance.

See www.altera.com/dsp for more information.

FEATURES:

- High-performance DSP blocks with multiplier, pipeline, and accumulate circuitry support >173 GMACS of DSP throughput
- 4 x the DSP block bandwidth of Stratix devices, up to 450 MHz
- New rounding and saturation support in a Q1.15 format in each DSP block
- Up to 9 Mb of memory in three block sizes and mixed-width data and mixed clock modules
- Supports an extensive IP portfolio and Nios® II processor implementations
- Optimized for hardware acceleration FPGA coprocessor applications
- Two DSP development kits deliver complete turnkey DSP development environment
  - DSP development board featuring a Stratix II EP2S60 device (Standard Edition) or EP2S180 device (Professional Edition)
  - Variety of analog and digital I/Os
  - 256 MB DDR2 DIMM, 1 MB synchronous SRAM, two EPCS64 devices
  - MATLAB/Simulink evaluation software, DSP Builder (one-year license), Quartus II DKE (one-year license)
  - Evaluation IP cores, system reference designs, and labs, cables, and accessories

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FPGAs for DSP

Accelerate the performance of your DSP system by using the XtremeDSP solution from Xilinx. Xilinx FPGAs are ideal for replacing your ASIC/ASSP or boosting the performance of your DSP processor.

Virtex-4 FPGAs for DSP
Virtex-4 FPGAs deliver the industry's highest performance and lowest power and cost for that performance. They are commonly used for radio-card and baseband functions in wireless infrastructure, MILCOM, and compute-intensive video imaging applications.

Highest performance: XtremeDSP Slices in Virtex-4 FPGAs deliver up to 256 GMACs performance using 512, dedicated 18 x 18-bit multipliers/48-bit adders, each capable of operating at 500 MHz.

Lowest power: With a power consumption of only 2.3 mW/100 MHz per XtremeDSP Slice, Virtex-4 FPGAs enable you to significantly reduce the power per channel in your communications or video systems.

Lowest cost for highest performance: The Virtex-4 SX platform delivers as many as 512, 500 MHz XtremeDSP Slices in a device that consumes half the silicon area of competing FPGAs.

Spartan 3/3E FPGAs for DSP
Starting at only $2 for 100 k gates, Spartan-3/3E FPGAs are ideally suited for compute-intensive applications where GMACs per dollar is important. Spartan-3/3E FPGAs enable you to build parallel DSP structures using 104, 18 x 18 embedded multipliers. Spartan-3/3E are ideal for high-volume consumer and automotive applications. In addition to signal processing, Virtex-4 and Spartan-3/3E FPGAs are ideal for lowering your system cost (through consolidating your system logic), bridging your serial or parallel buses, and implementing low-rate control functions using on-chip microprocessors such as IBM PowerPC, Xilinx MicroBlaze, and PicoBlaze. Designing your DSP algorithms onto FPGAs has never been easier, even if you don't write VHDL/Verilog. For information about Xilinx XtremeDSP Development Tools, see the Software section in this resource guide.

Visit www.xilinx.com/dsp for more information.

FEATURES:

- Virtex-4 for Highest Performance dsp – Up to 512, 500 MHz XtremeDSP Slices (18 x 18 multiply, 48-bit add)
- Virtex-4 for lowest power per channel – each XtremeDSP Slice consumes only 2.3 mW per 100 MHz
- Virtex-4 for lowest cost for high-performance DSP – More performance available in half the silicon area of competing FPGAs
- Spartan-3/3E for lowest cost FPGA-based DSP – Prices starting at $2 for 100 k gates in big volumes
- Spartan-3/3E for DSP performance acceleration in consumer/ automotive applications – Up to 104, 18 x 18 200+ MHz 18 x 18 multipliers
- XtremeDSP development tools to cater for hardware and non-hardware designers that prefer to use MATLAB/Simulink
- More than 60 XtremeDSP algorithms available from Xilinx and partners to help you finish first
- Multiple XtremeDSP development platforms available for standalone FPGA design or DSP coprocessing
- XtremeDSP education classes help you become proficient in the XtremeDSP design flow and design implementation techniques
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London, ON N6H 5S1 Canada
Tel: 519-690-0091 • Fax: 519-690-0092
www.microtronix.com

Embedded Module

The Firefly module combines programmable FPGA technology, 32-bit RISC processing power, and the μClinux OS into a small 2" x 2" footprint module. The EPM is an easy, low-cost, and quick way to add μClinux and/or FPGA-based processors to any embedded project. The heart of the EPM is an Altera Cyclone FPGA containing a Nios-II 32-bit RISC processor running at 110 MHz. The module can be pre-loaded with μClinux, a ROM disk, and various applications and drivers. Simply apply 3.3 V power to the power pins and you have a working uClinux environment for embedded designs. Create custom applications and device drivers using free IDE software.

FEATURES:

- Supports Altera Cyclone™ EP1C4 and EP1C12 devices
- FPGA configured with Altera Nios-II/f processor SOC
- Flash optionally pre-loaded with μClinux 2.6.11 kernel
- Provides 88 programmable GPIO pins, 16/32/64 MB SDRAM, 8/16/32 Flash and UART
- IP or MAC/PHY solutions for: USB 2.0, 10/100Base-T Ethernet
- FIFO interface available for TI and Analog Devices DSP processors

For more information, contact: sales@microtronix.com RSC #4201 @ www.DSP-FPGA.com/catalogrsc

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VMETRO Inc.

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1880 S. Dairy Ashford, Suite 400
Houston, TX 77077
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www.vmetro.com

PMC-FPGA03/F

The PMC-FPGA03 is a Xilinx XC2VP20/30/50 Virtex-II Pro based FPGA PMC module that interfaces directly to two banks of DDR SDRAM and three banks of QDR-II SRAM for high-performance, low-latency applications. Xilinx RocketIO channels are available either out of the front panel or the PMC connector as a build option. The PMC-FPGA03 communicates with a variety of Windows, VxWorks, and Linux host computers via an optimized 64bit/66 MHz PCI bus interface. The module is available in air-cooled and conduction-cooled variants. Fiber-optic options are also available. Example VHDL code blocks are provided to show how the PMC-FPGA03 resources can be used.

FEATURES:

- Xilinx XC2VP50 Virtex-II Pro FPGA
- Bandwidths up to 3.125 Gbps per port
- 64-bit user programmable data port (PMC user I/O P14)
- 2 x banks DDR SDRAM (64 MB per bank)
- 3 x banks QDR-II SRAM (up to 8 M x 18-bit per bank)
- 4 MB Flash memory

For more information, contact: info@vmetro.com RSC #4202 @ www.DSP-FPGA.com/catalogrsc

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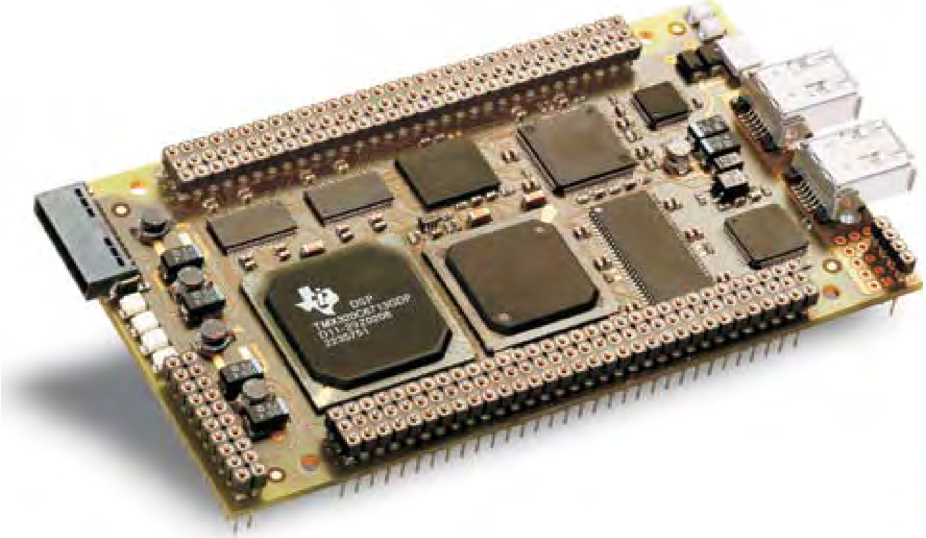

Micro-line C6713Compact
Embedded DSP Board:
TMS320C6713 DSP
with Virtex-II FPGA & FireWire

Ultra-compact UC1394a-1
Multi-chip module:
TMS320C5509 DSP with
Spartan-II FPGA & FireWire

Design Services

System integration and DSP algorithm design for TI DSP and Xilinx FPGA hardware systems

Data Acquisition

Multi-channel 12-, 14-, and 16-bit analog interface solutions for micro-line embedded DSP systems and TI DSKs

RSC #43 @ www.DSP-FPGA.com/rsc

Traquair Data Systems, Inc. Tel: 607-266-6000 Email: sales@traquair.com Web: www.traquair.com

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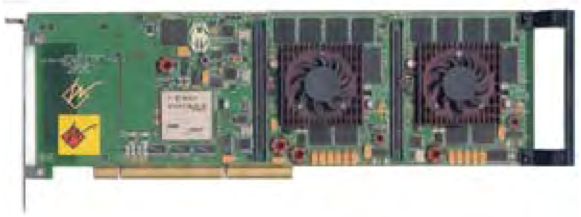
Your Source for Embedded Signal Processing

Annapolis Micro Systems, Inc.

Wildstar II PCI

Annapolis Micro Systems is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, digital signal processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications. Our ninth-generation WILDSTAR II Pro for PCI uses Xilinx's newest Virtex II Pro FPGAs for state-of-the-art performance. It accepts one I/O card in one, or up to two I/O cards in two PCI or PCI-X slots, including dual 1.5 GHz A/D converters, single 1.5 GHz A/D converter, Quad Fibre Channel 2, Quad 105 MHz, Quad Gigabit Ethernet, WILDSTAR Data Port (WSDP), FPDP, and LVDS. Our boards are on a large number of operating systems, including Win (NT, 2000, XP), Linux, DECAlpha, Solaris, IRIX, ALTIX, MacOS, and VxWorks. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. We offer training, including customized application development and customer support.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire is based on data flow and automatically generates distributed control fabric between cores. Our extensive IP and board support libraries contain more than 800 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules. WILDSTAR II Pro for PCI, with its associated I/O cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving savings in size, weight, power, person-hours, dollars, and calendar time to deployment.



FEATURES:

- One to two Virtex II Pro Xilinx FPGA processing elements – XC2VP70 or XC2VP100
- Up to 96 MB DDRII or QDRII SRAM
- Up to 256 MB DDR DRAM
- Programmable Flash for each processing element to share FPGA images
- Works with PCI or PCI-X backplane
- High-speed DMA multichannel PCI controller
- Host software: Win NT, 2000, XP, Linux, Solaris, MacOS, DECAlpha, IRIX, and ALTIX
- Full CoreFire board support package for fast, easy application development
- VHDL model, including source code for hardware interfaces
- Save time and effort and reduce risk with COTS boards and software
- Achieve world-class performance – WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

For more information, contact: wfinfo@annapmicro.com RSC #4401 @ www.DSP-FPGA.com/catalogrsc

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Your Source for Embedded Signal Processing

Annapolis Micro
Systems, Inc.

Wildstar II ProVME

Annapolis Micro Systems is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, digital signal processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing-intensive applications. Our ninth-generation WILDSTAR II Pro for VME uses Xilinx's newest Virtex II Pro FPGAs for state-of-the-art performance. It accepts up to two I/O cards in one VME64x slot, including dual 1.5 GHz A/D converters, a single 1.5 GHz A/D converter, Quad Fibre Channel 2, Quad 105 MHz, Quad Gigabit Ethernet, WILDSTAR Data Port (WSDP), FPDP, and LVDS. We host our boards on a large number of operating systems, including Win (NT, 2000, XP), Linux, DEC Alpha, Solaris, IRIX, ALTIX, MacOS, and VxWorks. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. We offer training, including customized application development and customer support. Develop your application very easily with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily and quickly build and test their algorithms on the real hardware that will be used in the field. CoreFire is based on data flow and automatically generates distributed control fabric between cores. Our extensive IP and board support libraries contain more than 800 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules. WILDSTAR II Pro for VME, with its associated I/O cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

FEATURES:

- One to three Virtex II Pro Xilinx FPGA processing elements – XC2VP70 or XC2VP100
- Up to 144 MB DDRII or QDRII SRAM
- Up to 384 MB DDR DRAM
- Programmable Flash for each processing element to store FPGA images
- Works with VME64x backplane
- High-speed DMA multichannel PCI controller
- Host software: Win NT, 2000, XP, Linux, VxWorks, Solaris, MacOS, DECAlpha, and SGI
- Full CoreFire board support package for fast, easy application development
- VHDL model, including source code for hardware interfaces
- Save time and effort and reduce risk with COTS boards and software
- Achieve world-class performance – WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

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innovation deployed

VPF1 Quad DSP

The VPF1 is a 6U VME64x signal processor that supports VITA 41 backplane switch-fabric communications via VXS over an enhanced VME P0 connector. The VPF1 comprises four processor nodes: two 1 GHz PowerPC 7447A CPUs and two Xilinx XC2VP70 Virtex II Pros. Each processor has fully distributed memory. The PowerPCs each have access to 256 MB of DDR SDRAM, and the FPGAs are directly coupled to multiple banks of QDR SRAM in addition to local DDR SDRAM. Each FPGA supports multiple inter-node communication channels via the RocketIO devices native to the Virtex II Pro. Four channels connect the two onboard FPGAs, and the remaining eight go off-board facilitating scalable, point-to-point processing. Each of these channels can be routed at speeds up to 3.125 Gbps between VPF1s or other compatible VXS cards. A PMC site, GigE, and VME P2 directly connected to an FPGA facilitate high-speed IO.

VxWorks and TimeSys Linux Board Support Packages (BSPs) can be supplied to run industry standard operating systems on the VPF1's PowerPCs. Routines in the BSP can configure the local FPGAs. VHDL source code is supplied to communicate with local memory and other directly attached IO. Example firmware and extensive documentation enable end-user applications to be quickly configured for use on the VPF1.

VPF1s are available in air-cooled or conduction-cooled builds, enabling easy migration from development to production.

FEATURES:

- 2 x PowerPC 7447 CPU nodes
- 2 x Xilinx Virtex-II Pro FPGA nodes
- 8 x 2.0-3.125 Gbps off-board serial communications channels
- Ethernet, RS-232, and RS-422
- 64-bit, 66 MHz PMC site for local I/O
- Air-cooled and rugged conduction-cooled build variants
- Optimized VSIPL DSP libraries
- VXS compatible
- VxWorks, Linux, and Gedae support

For more information, contact: info@vmetro.com

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AMIRIX Systems Inc.

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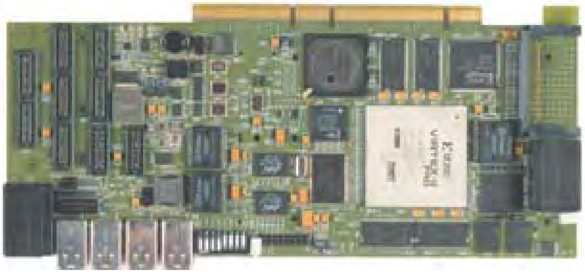
77 Chain Lake Drive
Halifax, NS B3K 4V8 Canada
Tel: 902-450-1700 • Fax: 902-450-1704
www.amirix.com

AMIRIX FPGA Boards

The AMIRIX AP100/1000/4000 PCI platform FPGA development boards are PCI cards with a Xilinx Virtex-II Pro™ or Virtex-4™ FX FPGA that provide an instant, "out-of-box" system for developing embedded FPGA System-on-Chip (SoC) solutions. The boards come configured as a single board computer with monitor software and Linux OS, and also provide an advanced design starting point to improve time to market and reduce development costs. Additional platform modules and accessories are available to support the development of programmable systems. Amirix also offers competitively priced custom derivative designs through its supporting design services.



FEATURES:

- Supports devices: XC2VP7, XC2VP20, XC2VP30, XC2VP70, XC2VP100, XC4VFX60, and XC4VFX100
- Memory: DDR SDRAM, DDR-II SDRAM, SRAM, QDR-II SRAM, Program Flash, Configuration Flash, SystemACE with CompactFlash
- Networking: 10/100Base-T Ethernet controller, 10/100/1000Base-T Ethernet, RS-232D, MGT with SMA, SFP, and XFP support
- Support for 1-8 x PCI Express and up to four InfiniBand connectors
- 32/64-bit, 33/66 MHz; accommodates PCI Rev 2.2 add-in card

For more information, contact: request.info@amirix.com RSC #4701 @ www.DSP-FPGA.com/catalogrsc

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DSP-FPGA.com Product Resource Guide 2005 Prototyping boards

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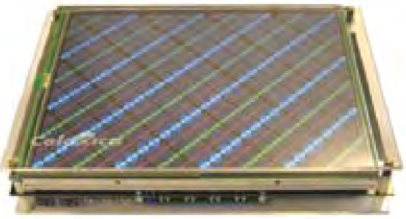
Acceleration Cards

Celoxica algorithm acceleration platforms are based on the latest FPGA devices from Altera and Xilinx and provide all the features needed to prototype complex DSP-based systems.

These high-performance cards, designed for high-speed video and data applications, are optimized for throughput and integration of soft-core microprocessors. The cards come in both desktop and PCI configurations.

In addition, Celoxica provides board support libraries for their powerful C-based synthesis tools to offer a complete algorithm-to-prototype environment from C to FPGA. Software programmers can access all board features using a C-based API.



FEATURES:

- High-performance FPGA devices and peripherals for acceleration of high-speed signal processing applications
- Designed to smoothly off-load processors with FPGA hardware accelerators
- Software programmable using Celoxica C-based synthesis tools
- Supported by extensive software API and IP libraries

For more information, contact: sales@celoxica.com RSC #4702 @ www.DSP-FPGA.com/catalogrsc

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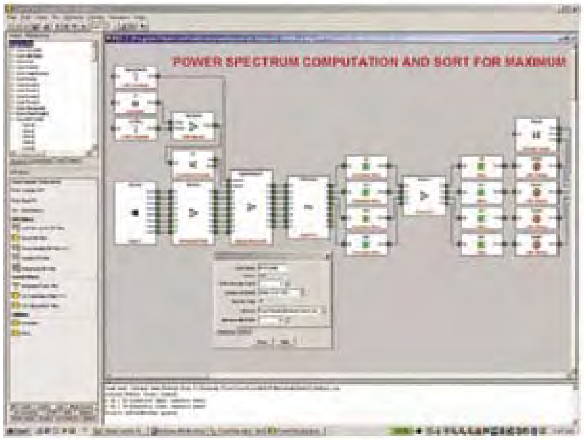
CoreFire FPGA

Develop your application very quickly and easily with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily and quickly build and test their algorithms on the real hardware that will be used in the field. Use CoreFire's graphical interface to drag and drop library elements onto the design window. Modify your input and output types, numbers of bits, and other core variables by changing module parameters with pull-down menus. The modules automatically provide correct timing and clock control. Insert debug modules to report actual hardware values for hardware-in-the-loop debugging. Hit the Build button to check for errors and as-built core sizes and to build an encrypted EDIF file. Use the Xilinx ISE tool to place and route each FPGA design. Modify and use the jar file or the C program created by the CoreFire Build to load your new file into your WILDSTAR II and I/O card hardware. Use the CoreFire Debugger to view and modify register and memory contents in the FPGA, and to step through the data flow of your design running in the real physical hardware. Our extensive IP and board support libraries contain more than 800 proven, reusable high-performance cores, including FIR and CIC filters, a channelizer, and the world's fastest FFT. We support conversion between data types: bit, signed and unsigned integers, single precision floating point, integer and floating point complex, and arrays. A few of the newly added array cores include array composition and decomposition; slice, parallelize, serialize, repack, split, merge, reorder, rotate, and concatenate transformations; matrix math, sliding windows, and convolutions. The combination of our COTS hardware and CoreFire enables our customers to make massive improvements in processing speed while achieving savings in size, weight, power, person-hours, dollars, and calendar time to deployment.



FEATURES:

- Data-flow-based – automatically generates intermodule control fabric
- Drag and drop graphical interface
- Work at high conceptual level – concentrate on solving algorithmic problems
- Hardware-in-the-loop debugging
- More than 800 modules incorporate years of application experience
- Reduce risk
- Save time to market
- Save development dollars
- Easily port completed applications to new technology chips and boards
- Training and custom application development available
- Achieve world-class performance – WILD solutions outperform the competition
- Annual node locked or networked license; includes customer support and updates

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CtoFPGA Synthesis

Celoxica provides complete design environments for synthesis of C algorithms to FPGA hardware from both Handel-C and SystemC. Celoxica is the leading supplier of C-based design and synthesis tools, specializing in digital imaging and signal processing applications.

Celoxica C-synthesis produces optimal design partitions and quality results, maximizes design productivity, and directly implements complex DSP software to FPGA and RTL.

Celoxica's proven technology has been used in thousands of designs to accelerate system performance, cutting design cycles in half and turning software algorithms into FPGA silicon.

FEATURES:

- Direct synthesis from Handel-C (synthesizable ANSI-C) or SystemC models to FPGA gates
- Fast cycle-accurate simulation of system models in C, C++, Handel-C, or SystemC; co-simulation with RTL and MATLAB models
- Rapid partioning of algorithms between processors and FPGA hardware; integration with popular processors
- Generation of human readable RTL models and integration with common ASIC tool flows

For more information, contact: sales@celoxica.com RSC #4901 @ www.DSP-FPGA.com/catalogrsc

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First Silicon Solutions

Your Source for Embedded Signal Processing

4000 SW Kruse Way Place, #3-210
Lake Oswego, OR 97035
Tel: 503-489-0311 x103 • Fax: 503-489-0315
www.fs2.com

System Navigator

The System Navigator supports the Altera® Nios® II embedded processor. The user can build a Nios II device with an On-Chip Instrumentation (OCI®) debug block. The OCI provides powerful trace, triggering, and performance analysis features for faster system and software debug and testing.

The System Navigator is contained in a compact chassis that connects to the Nios II target system using a 10-pin JTAG debug connector. The system runs on a Windows® 2000/XP PC over a USB 2.0 interface or optional 10/100Base-T Ethernet connection.

FEATURES:

- Complete debug solution for Nios II processors
- On-chip and off-chip trace capture options
- Source-level debugging with Altera Nios II IDE
- Performance monitor features two 40-bit counters
- Enables faster device and Flash programming
- Software breakpoints and hardware triggers

For more information, contact: info@fs2.com RSC #4902 @ www.DSP-FPGA.com/catalogrsc

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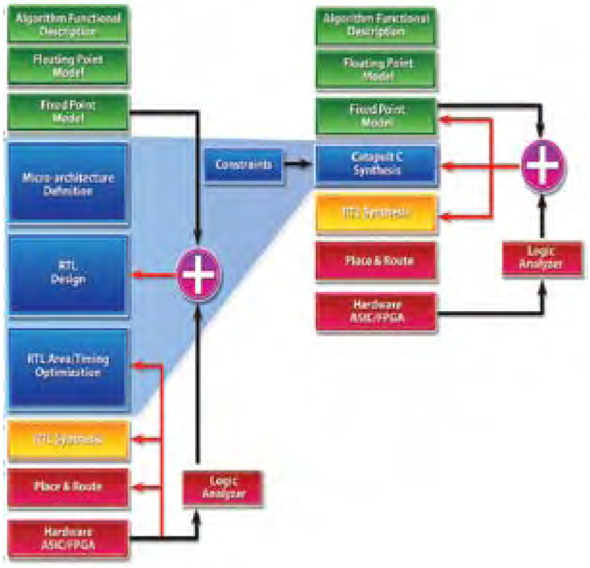
Catapult C

Catapult™ C Synthesis is a customer-proven algorithmic synthesis environment that automatically generates RTL from pure ANSI C++ up to 20 x faster than manual methods. Using pure C++ to describe functional intent, engineering teams move up to a more productive abstraction level for designing complex, compute-intensive ASIC or FPGA hardware.

Combining interface synthesis technology with design architecture analysis and incremental optimization allows designers to produce hardware designs that meet or exceed hand-coded quality. Catapult's new extension to SystemC verification provides customers with an automated algorithmic synthesis-to-verification flow using transaction-level models for system simulation. Catapult C Synthesis unites the system-level and hardware design domains, and when combined with Mentor Graphics® Questa™ simulation tools, lays the foundation for next-generation Electronic System Level design.



FEATURES:

- Pure ANSI C++ synthesis
- Technology independent source
- Micro-architecture and interface incremental analysis and optimization
- Error-free RTL creation
- Faster, more reliable verification
- Commercial deployment: more than 30 chips in production

For more information, contact: sales@mentor.com RSC #5001 @ www.DSP-FPGA.com/catalogrsc

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Precision Synthesis

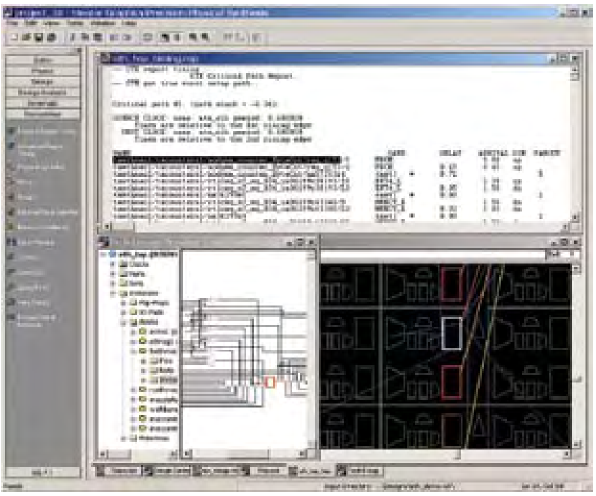
Combining easy-to-use automated synthesis with expert-level interactive optimization and control, Precision® Synthesis is the tool of choice for FPGA developers at every level to start designs right, improve designs quickly, and meet project requirements.

This complete RTL and physical synthesis environment delivers high productivity and high quality results within a vendor-independent methodology. Powerful debug/analysis, project management, and inferencing capabilities, along with placement reuse and modular design flows, help shorten design cycles, improve performance, and create high-quality FPGA designs.

Traditional RTL synthesis is enhanced with physically aware retiming, replacement, replication, and re-synthesis algorithms. Optimizations are focused on potential bottlenecks like FSMs, cross-hierarchical logic, and paths with excessive combinational logic. Retiming balances logic across register boundaries to improve overall design performance, hierarchy optimization minimizes logic between modules, and pipelining moves registers into multipliers.

You can cross-probe from elements in any report to the RTL source code, and design schematics or physical layout. Precision Synthesis also automatically infers memory, DSP, and other technology-specific elements. The built-in PreciseTime analysis tool generates interactive timing reports from any port, pin, or instance. You can initiate timing queries throughout the user interface, including selected objects in the schematic viewer. RTL schematics help you determine the impact of coding styles, and detailed technology schematics depict device-specific resource utilization. The PreciseView layout editor and diagnostic tool makes timing data readily available. Edits are checked for legal placements in real time to avoid design rule violations.

Precision Synthesis supports VHDL, as well as Verilog 2001 and SystemVerilog. It runs on Windows, Linux, and Solaris, and supports devices from all FPGA vendors.



FEATURES:

- Advanced FPGA synthesis technology helps FPGA designers to start designs right, improve designs quickly, and meet requirements
- Integrated RTL and physical synthesis environment enables higher productivity and quality of results
- FPGA device- and vendor-independent methodology enables selection of the right device for each design and reduces development cost
- Intuitive user interface with comprehensive project management capabilities improves designer productivity
- Incremental debug/analysis environment with cross-probing identifies and fixes problems early in the design process
- Fully automated technology inferencing (memories, DSP blocks, and so forth)
- Advanced design flows reduce the number of iterations
- Retiming algorithm moves registers across logic to improve performance
- Acts as a complete FPGA design cockpit with tight integration to all FPGA vendors' place-and-route tools
- Language neutrality supports any combination of VHDL, Verilog, and SystemVerilog

For more information, contact: sales@mentor.com RSC #5101 @ www.DSP-FPGA.com/catalogrsc

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Mentor Graphics®

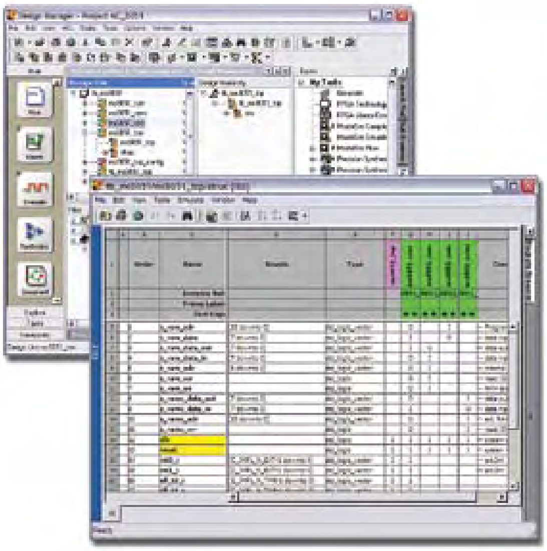
HDL Designer

Mentor's HDL Designer™ is a complete and integrated design environment for creating and managing VHDL, Verilog, SystemVerilog, and mixed-language designs. Built from the ground up to support complex FPGA and ASIC designs in a collaborative environment, the enterprise-level HDL development platform gives every member on your team access to advanced techniques that can help to quickly create accurate code from scratch, or to understand existing code/IP.

Simply drag and drop existing code into a design and start creating your own custom blocks of logic using a variety of efficient editors. Partition your design for team members using a block diagram or a spreadsheet view, and have the tool generate structural RTL automatically. Then use the text editor or finite state machine editor to define your logic and generate code. The built-in DesignChecker tool ensures that the code fully meets your design rules and, thus, prevents surprises downstream.

HDL Designer is fully integrated with the industry-leading simulation (ModelSim®), synthesis (Precision® Synthesis), and PCB design (I/O Designer™) solutions from Mentor Graphics, as well as a wide range of FPGA device vendor tools. This allows teams to move seamlessly through design flows, efficiently manage resultant data, and drastically shorten the number and length of iterations. When it comes time to create documentation or to build interactive websites for design reviews, HDL Designer can create accurate graphical representations of the source code and create a complete interactive website for your design at the touch of a button.

HDL Designer thus enables companies to scale both organizational productivity as well as engineering productivity by providing an impressive array of technologies focused on design creation, analysis, checking, documentation, and management capabilities within a single tool. Ultimately, the value you extract by using HDL Designer is that it maximizes your FPGA/ASIC design productivity.



FEATURES:

- Enables scalable RTL development across distributed design teams, spanning FPGAs to multimillion gate ASICs
- Creates and manages complex Verilog, VHDL, SystemVerilog, and mixed-language ASIC and FPGA designs
- Design in a way you're most comfortable with, by selecting from various textual, tabular, or graphical editors to generate code
- Automatically produce graphical and HTML documentation for design reviews, archival, and reuse
- Manage and interact with all project data, optionally under version control
- DesignChecker™ delivers advanced static analysis up front in the design process to help create "correct-by-construction" code
- Enables practical design reuse through rapid evaluation and visualization of existing code and easy deployment of IP
- Designers can use a favorite HDL simulator and synthesis engine, creating an easier, more productive HDL design process
- Integrates other design tools easily with TCL, to run from within the HDL Designer environment

For more information, contact: sales@mentor.com RSC #5201 @ www.DSP-FPGA.com/catalogrsc

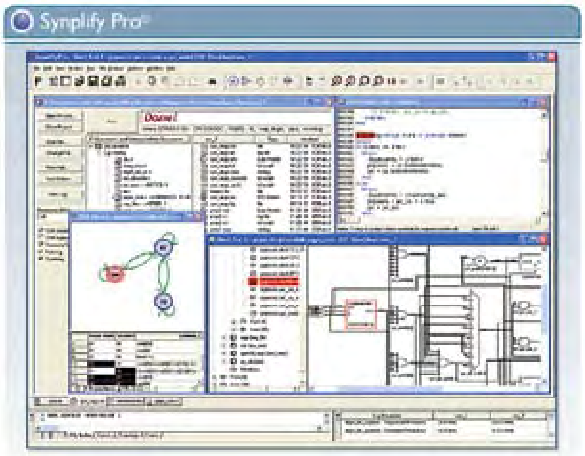
Synplicity, Inc.

600 W. California Avenue
Sunnyvale, CA 94086
Tel: 408-215-6000 • Fax: 408-222-0268
www.synplicity.com

Synplicity
Simply Better Results

Synplify Pro® Tool

High quality of results, fast runtimes, and ease of use has made the Synplify Pro advanced FPGA synthesis solution the industry's most popular and robust FPGA synthesis product. The Synplify Pro product can achieve the highest circuit performance through its automatic retiming capability and advance Finite State Machine exploration technology. As the only truly timing-driven FPGA synthesis tool, this solution has the ability to automatically optimize for area (cost) once timing constraints have been met. The Synplify Pro solution is the most widely used FPGA synthesis product and is endorsed by leading FPGA vendors such as Actel, Altera, Lattice Semiconductor, Quicklogic, and Xilinx.



FEATURES:

- #1 FPGA synthesis solution
- Interactive timing analysis
- Compatible with popular formal verification tools
- Lightning-fast compile times
- Comprehensive language support: Verilog, VHDL, mixed language
- Third-party tool integration

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Amplify® Family

Synplicity's Amplify family of custom structured/platform ASIC synthesis products are the only custom physical synthesis solutions that target Fujitsu's AccelArray™ structured ASIC, LSI Logic's RapidChip® platform ASIC, and NEC Electronics' ISSP™ structured ASIC architectures. The Amplify family of products uniquely allows the front-end designer to perform a single-pass hand-off to their vendor with timing pre-closed – no costly iterations between customer and vendor are necessary to resolve timing issues. Designers achieve working silicon in a 6-9 month cycle, allowing them to get new features to market fast. This time saving translates to huge project cost savings for 90 nm and below designs. The Amplify family of products currently consists of the Amplify AccelArray Pro physical synthesis tool customized for Fujitsu's AccelArray structured ASIC architecture; Amplify RapidChip and Amplify RapidChip Pro physical synthesis tools customized for LSI Logic's RapidChip platform ASIC architecture; and Amplify ISSP Pro physical synthesis tool customized for NEC Electronics' ISSP structured ASIC architecture.

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FEATURES:

- Integrated physical synthesis
- Architecture-aware floor planning and design analysis
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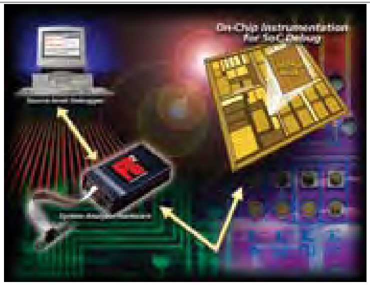
The FS2 Logic Navigator™ is an On-Chip Instrumentation (OCI®) trace and debug tool that provides logic analysis capability to Actel FPGA internal logic. It supports Actel® Flash-based FPGAs, including ProASIC and ProASICPLUS, and Antifuse devices (MX, SX, and AX) providing an intuitive and easy way to view internal signals and debug the logic design. It can simultaneously trace and trigger up to 256 signals in the FPGA fabric with support for up to 4096 total nodes during the debug session.


On-Chip Instrumentation for SoC Debug

FEATURES:

- OCI technology for trace and triggering on signals in Actel FPGA devices
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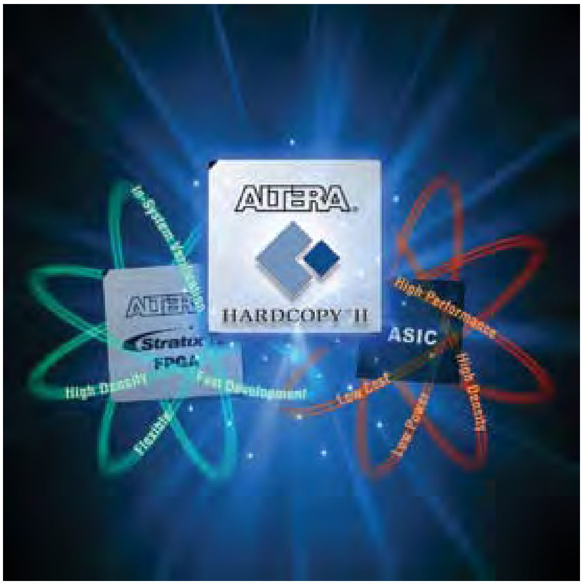
HardCopy II Structured ASICs

Altera's 90-nm HardCopy® II family delivers the industry's only FPGA-prototype-to-structured-ASIC design flow. Designers use Altera's high-density, high-performance Stratix® II FPGAs to develop and verify a design before committing to silicon. The product development flexibility and time-to-market benefits of HardCopy II structured ASICs are unparalleled by any other offering in the market. Ideal for high-volume designs with prices starting as low as US$15, the HardCopy II family gives you a competitive edge in DSP applications.

HardCopy II structured ASICs deliver 350 MHz system performance, 8.8 million bits of memory, and up to 2.2 million ASIC gates for logic prototyping. Designers create their DSP designs in Stratix II FPGAs, which have flexible DSP blocks that can implement fast, arithmetic-intensive applications such as image processing, wireless communications, military broadcast, and medical. Each DSP block has dedicated multi-width multipliers, available in 36 x 36, 18 x 18, or 9 x 9 widths to implement DSP algorithms and functions, including filtering, video and image processing, correlation, transforms, encryption, and error correction. Stratix II FPGAs offer high DSP throughput to meet the requirements of emerging standards and protocols, such as JPEG2000, MPEG-4, H.264, 802.16x, CDMA2000, 1xEV-DV, HSDPA, and W-CDMA.

When the design is complete, Altera's HardCopy Design Center migrates the design to a HardCopy II structured ASIC for volume production. The end result is a structured ASIC that is functionally equivalent and pin-compatible with the Stratix II prototype used to verify the design, with up to twice the performance and half the core power consumption, all at as little as one-tenth the cost.

HardCopy II structured ASICs are supported by Altera's Quartus® II software design flow and EDA tools typically used in FPGA and ASIC design flows, minimizing additional training time and expenses.



FEATURES:

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Turning Software into Silicon

C synthesis accelerates the creation of technology-independent DSP hardware

By Shawn McCloud, Product Line Director,
High-Level Synthesis, Mentor Graphics

Advanced C/C++ algorithmic synthesis methodologies enable a new possibility for custom, high-performance DSP hardware. Starting with a technology-independent sequential description in pure ANSI C/C++, this development process gives DSP hardware designers a safe and fast path to RTL descriptions. A single ANSI C/C++ source can create small compact designs (serial) to fast, high-performance designs (parallel), allowing optimal designs for the exact system requirements (performance and area) and tuned to any ASIC or FPGA technology. In addition, automation of RTL creation yields up to 20x faster design time and up to 60 percent fewer bugs versus hand-coded RTL, providing a safer, faster, and more reliable design flow.

DSPs vs. FPGAs vs. ASICs

Having evolved for decades, the discrete DSP realm now comprises tailored design environments, offering a complete value chain of stable applications and flows. Working with off-the-shelf DSPs is essentially a programming function, relying on the software engineer's C/C++ or MATLAB coding expertise to achieve desired functionality. Probably the most important factor that draws the mainstream community to these discrete devices is their ease of use and programmability.

This rosy picture is changing, however. Users have a robust design solution but, unfortunately, the massive increase in processing required for next-generation, compute-intensive applications, such as wireless communication and image processing, has created a gap between off-the-shelf DSP performance and market needs. In many cases, discrete DSPs are simply running out of steam to serve the new communications, multimedia, and consumer applications. In recent years, users have increasingly looked toward alternative solutions ranging from ultra high-performance, full-custom ASICs to highly flexible general-purpose CPUs. Somewhere in the middle are FPGAs, providing a cost-effective balance (Figure 1) between programmability and high performance. With their processing flexibility ranging from serial to parallel computing, and now containing highly specialized DSP macros and memories, FPGAs have the potential to become an attractive option in which to implement DSP algorithms.

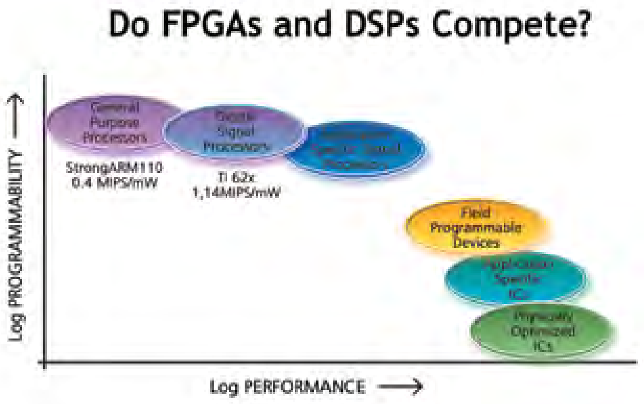

Figure 1

Each platform has certain benefits and limitations. On one extreme, the pure software approach implemented in discrete DSPs is mature, flexible, and relatively easy to use but offers limited instruction-level parallelism. On the other extreme, ASIC implementations offer custom performance and high volume pricing benefits but traditionally constitute a much greater design effort and soaring NRE costs. Demonstrating some of the value from both extremes, FPGA hardware supports reprogrammability and architecture flexibility in terms of spatial and temporal parallelism (via repetition and pipelining) but lacks ease of programming since design entry is in RTL versus the DSP program domain of ANSI C/C++.

The catch-22 situation is that designers want the programming flexibility of the discrete DSPs and the performance flexibility available in FPGAs. How can they combine the best of both worlds? And, more importantly, what are their options if the application calls for the use of an ASIC implementation? Optimal implementation of DSP algorithms, therefore, requires a serious rethinking about how to approach the overall design flow when transforming algorithms into hardware, via either the ASIC or FPGA route. In the end, choosing the path of technology independence could mean the difference between success and failure.

Pure ANSI C/C++ algorithmic synthesis bridges design gap

To use Register Transfer Level (RTL) to create hardware implementations for complex DSP algorithms, design teams must iterate through several steps, including micro-architecture definition, handwritten RTL, and area/speed optimization through RTL synthesis. This manual process is slow and induces up to

60 percent of the bugs found in RTL due to a misintended design from original specification. In the final result, both the micro-architecture and technology characteristics become hard-coded into the RTL description. This effect severely limits the notion of RTL reuse or retargeting for real applications, and leads to overbuilt designs and wasted silicon.

New DSP-specific flows enable algorithmic design at a higher level of abstraction than RTL (Figure 2). Although some C synthesis tools have been available for some time, none have delivered the necessary ease-of-use and quality of results until now. The latest breed of advanced C-based tools, such as Catapult™ C Synthesis from Mentor Graphics, takes industry standard, pure ANSI C++ as input and automatically produces RTL based on user-provided design goals. This approach closes the conceptual gap between algorithm designers modeling in pure ANSI C or C++ and hardware designers working at the RTL abstraction level (Figure 3). Both sides benefit because of:

- Technology-independent source (a critical differentiator, since it enables designers to choose between ASIC or FPGA implementations)
- Ability to incrementally explore and optimize implementation architecture (providing a design architecture and RTL tuned to system requirements without the need for hand-coded RTL)
- Automatic, fast creation of RTL code (providing an accurate flow that produces up to 20X faster design time and up to 60 percent fewer bugs)

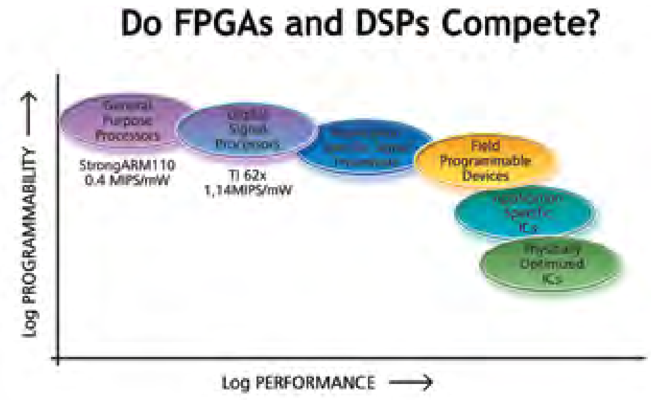

Figure 2

More importantly, the ability to select fundamentally superior platform-independent micro-architectural alternatives enables designers to create hardware designs of better quality than traditional RTL methods. Using this methodology, hardware designers can easily perform "what if" tradeoffs evaluating area, latency, throughput, and clock frequency for each micro-architecture, all while leaving the original pure ANSI C/C++ source unchanged.

Larger, faster designs are increasingly common in the DSP realm, which implies prolonged simulation and synthesis cycles. It has become imperative to fix as many code errors as possible prior to simulation and synthesis, using the design checking capabilities in interactive HDL visualization tools. Moreover, verification takes significantly longer than design development because of the limited speed of RTL simulators and the time to manually create an RTL test bench. Advanced design verification flows, with support of industry-standard simulation tools, are now addressing rapid algorithm validation and verification by mixing the high-speed characteristics of pure ANSI C/C++ with HDL like modeling benefits found in SystemC and SystemVerilog.

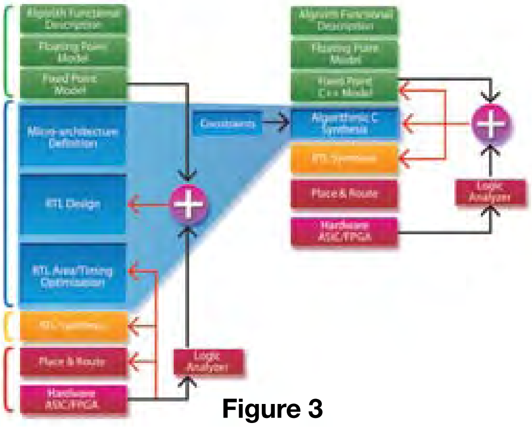

Figure 3

Bringing DSP up to speed using FPGA or ASIC

Algorithmic synthesis must also take into consideration technology-specific characteristics of RTL synthesis to be fully effective. For example, algorithmic synthesis must be aware of high-performance operations available in some FPGAs such as dedicated block multipliers, multiply/accumulate macros, pipelined operations, and special memory architectures. For ASICs, algorithmic synthesis must leverage the wide range of operator architectures available in RTL synthesis ranging from high-performance booth encoded parallel multipliers to area efficient bit-serial multipliers.

The key is knowledge-based synthesis tailored to the RTL synthesis tool. As such, algorithmic synthesis must be keenly aware of the inherent characteristics of RTL synthesis tools. Tight integration between algorithmic synthesis and RTL synthesis ensures timing closure in the back-end as well as accurate performance and power estimates in the front end.

Challenges and opportunities abound

All said and done, there are still limitations and challenges ahead. While FPGA devices are bigger than ever before, they nonetheless are still constrained by size. The largest algorithms admittedly will not fit onto current FPGAs. FPGA cost and power consumption are still major issues in consumer applications, where DSP applications have major impact. Technology-independent solutions such as algorithmic C synthesis provide the inherent flexibility to target critical DSP algorithms between discrete DSP, ASIC and FPGA implementations, a critical success factor since application segments dictate market cost, performance, and flexibility requirements. Using the innovative, technology-independent solutions now becoming available, the design community can stay ahead of the competitive curve and fully exploit the unprecedented opportunities ahead.

For more information, visit the Mentor Graphics website at www.mentor.com.

Software comes of age

By Dan Dodge, CEO and CTO, QNX Software Systems

QNX SOFTWARE SYSTEMS

The importance of software has grown tremendously throughout the last 25 years. Without software, life as it is today would grind to a halt. There would be no Web, no e-commerce, and no way to manage today's incredibly complex business and manufacturing environments. In biological terms, software has become a cornerstone species: everything else benefits from it, everything else depends on it. But with that importance comes immense responsibility – a responsibility that the software development industry is failing to embrace.

It's time, then, for software companies to raise the bar on reliability and security by creating designs that can intelligently defeat both internal faults and external threats. The very ability of software to drive innovation hangs in the balance.

The fact is, software is like a teenager on the cusp of adulthood. Although it has grown in the last few years, it is just beginning to tap into its true potential. To achieve that potential, companies that create software must ramp up their efforts to ensure that poor design, bad code, or malevolent hackers don't compromise the products they unleash upon the world. Developers must assume that, in today's increasingly complex and highly connected environments, the unexpected will occur. From day one, they must embed the appropriate safeguards into their applications. The world – with its profound reliance on software – will demand no less.

Moving beyond the Maginot mindset

The software industry's situation today is reminiscent of the 1930s, when France completed a masterpiece of military engineering called the Maginot Line. Bristling with more than 50 forts, it provided the country's eastern frontier with a virtually impregnable line of defense until one day when the German army simply walked around it.

Sadly, when it comes to software reliability and security, the "Maginot mindset" reigns supreme. Engineers are designing applications, even OSs, with the tacit – and erroneous – assumption that bugs and malware won't get around the verification efforts, authentication protocols, and other protective measures that constitute software's Maginot Line. Admittedly, however, most engineers employ these measures halfheartedly, if at all. Think log fences rather than stone fortresses.

The reality on the ground is very different. Hard-to-detect programming errors make their way past test and verification teams and into final product – as anyone who has experienced the Blue Screen of Death will attest. Viruses and hackers, meanwhile, can infiltrate a networked system, using tactics that the system's designers didn't – or perhaps couldn't – anticipate. As systems everywhere become more software-intensive and more connected, the potential for such vulnerabilities will only increase. And not just on desktops and servers, but in billions of embedded devices as well.

What's at stake here isn't simply the protection of applications or data. Rather, the very ability of software to usher in the next wave of innovation hangs in the balance.

Take the automotive industry, for instance. A new generation of in-car telematics and infotainment devices is hitting the streets, offering everything from CD ripping to 9-1-1 emergency dialing to real-time traffic updates. To succeed, such devices must connect to the outside world, whether to download updated Bluetooth stacks or to access new multimedia codecs. Moreover, consumers will expect these systems to interact with a variety of other personal devices, including MP3 players, USB storage keys, and digital media cards.

The question is, how can critical software components in such an environment be updated safely? And how can the existing behavior of the telematics device be guaranteed, even when it downloads software or data from a potentially untrusted source?

Web services pose similar challenges. On the one hand, Web services hold immense potential for simplifying tasks such as monitoring, configuring, and provisioning remote devices, from industrial controllers to telematics systems to software-defined radios built on platform FPGAs. At the same time, this connectivity opens the possibility that potentially malevolent parties or applications will infiltrate such devices.

Expecting the unexpected

Fortunately, solutions are at hand. There are approaches to persistent storage, for instance, that can place "bubbles" around files and memory, thereby preventing unauthorized access by rogue processes. Likewise, there are advanced approaches to partitioned scheduling that can prevent poorly written or malicious code from starving critical tasks of CPU time. Using such approaches, a device can continue to behave correctly, even if it has downloaded code that is trying to launch a denial-of-service attack.

In addition, let's not forget protected-mode computing. It's a critical first step to ensuring the reliability of virtually any software-rich device. Yet, many device designers and application developers, especially those in the embedded space, still fail to embrace memory protection even though it can contain faults and limit errant processes from corrupting the code or data of other pro. sors, including those embedded in platform FPGAs, such protection is becoming increasingly affordable. In fact, developers of connected devices must seriously ask whether they can afford not to use it.

Moreover, developers should not presume such techniques serve as a substitute for best development practices. Developers must also employ every tool and methodology at their disposal to ensure their code is clean, modular, efficient, thoroughly tested, and well-protected. The problem is, however, no one has developed a method to create code that is 100 percent bug-free. And no test suite can possibly exhaust every scenario that a complex software system may encounter, partially because the number of potential scenarios can, in such systems, be almost limitless.

Thus, despite all reasonable precautions, faulty code or disgruntled hackers can find their way into systems. Rather than pretend this won't happen, it would seem imperative that software developers, designers, and managers adopt a "mission critical" mindset and build systems to contain – and intelligently recover from – such problems. Never assume the fortifications will hold.

In short, developers must adopt a two-fold plan. First, do everything possible to ensure problems won't occur. Second, assume problems will occur anyway, and take appropriate measures. As a cornerstone species, software is too important for developers to create it any other way.

Driving innovation

Until recently, advancements in computing have been riding on the back of hardware and chip design. But as Moore's Law slowly loses steam, software is moving to center stage. From here on, it is software that will drive innovation – provided it's designed with the rigor, forethought, and safeguards commensurate with its burgeoning importance. Goodbye bloatware and Blue Screen of Death. Hello best practices and self-healing systems.

For more information, visit the QNX website at www.qnx.com.

Self-healing SOCs

With the advent of FPGAs that incorporate MMU-enabled processor cores, even FPGA-based System-On-Chip can use memory protection to contain, and recover from, potential software faults. For instance, the Xilinx Virtex-II Pro and Virtex-4 FX FPGAs can both incorporate multiple PowerPC cores, allowing systems designers and software engineers to leverage a variety of memory-protected operating systems such as the QNX Neutrino RTOS.

Memory protection offers benefits during development and at runtime. During development, common coding errors can cause a program to accidentally overwrite memory used by other programs, including the RTOS kernel. If the overwrite touches memory that isn't referenced again until much later, pinpointing the source of the problem can take long hours of debugging. With an MMU enabled, however, the RTOS can abort the process at the instant the violation occurs and provide immediate feedback to the programmer. The RTOS can also indicate the location of the errant instruction or position a symbolic debugger directly at that line of source code.

At runtime, the RTOS can catch such errors and pass control to an application process called a software watchdog. The watchdog can then restart the rogue process and, if required, any related processes. (The system designer can determine exactly which actions the watchdog should take, based on the failure scenario.) The watchdog can also generate a process dump file that programmers can subsequently debug offline. As a result, a deployed system can survive intermittent software failures without downtime and without users realizing that the system has, in effect, healed itself of a potentially fatal programming error.

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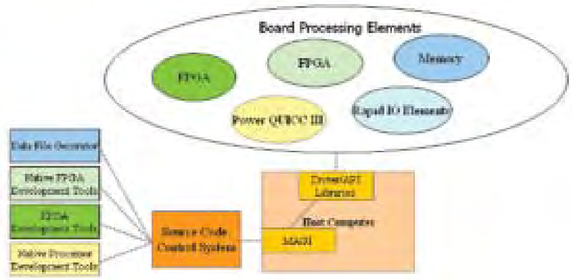
VTI-MAGI DDE

Heterogeneous computing environments present a daunting task for system engineers and algorithm developers. Programming and timing needs of all processing elements contained in the system as well as system data flow must be addressed. The typical programming model for a heterogeneous computing platform employs a "one board/system, many downloads" model. The number of download files can be in the hundreds, and when your processing needs require real-time reprogramming of the system, the number of download files could increase tenfold. This programming model poses significant obstacles to repeatability and makes software and algorithm reuse nearly impossible. The solution to this complex problem lies in the combination of a source code control system, board/system element programming, and board/system operational control. The MAGI Development and Deployment Environment (DDE) was designed to meet these needs. MAGI uses a "one board/system, one package" model. This model addresses the complexities of managing and deploying application programs on heterogeneous computing platforms. The MAGI programming model creates a "download package" for the board/system. The download package contains all files needed to program all elements of the board/system, thus the "one board/system, one package" model. The MAGI DDE provides total control over the application development process, facilitating software reuse and rapid deployment of new system configurations. MAGI provides a uniform interface for the application developer to manage the application library, test new algorithms on the hardware, and provide automated system configuration for reliable, repeatable results.



FEATURES:

- Single viewpoint for the board/system for fast migration to system deployment
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- Integration and algorithm development
- Layered architecture provides simplified feature additions and modifications
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DSP Builder

Altera's DSP Builder development tool provides everything needed to design DSP applications in Altera's programmable logic devices. It integrates high-level algorithm and Hardware Description Language (HDL) development tools by combining the algorithm development, simulation, and verification capabilities of The MathWorks MATLAB and Simulink system-level design tools with VHDL synthesis, simulation, and Altera® development tools into a single design environment. DSP Builder shortens DSP design cycles by helping designers create the hardware representations of DSP designs in an algorithm-friendly development environment. The existing MATLAB and Simulink blocks can be combined with DSP Builder blocks and Altera's Intellectual Property (IP) MegaCore® functions to link system-level design and implementation with DSP algorithm development. In addition, this design tool allows system, algorithm, and hardware designers to share a common development platform.

Designers can use the blocks in DSP Builder to create a hardware implementation of a system modeled in Simulink in sampled time. DSP Builder contains bit- and cycle-accurate Simulink blocks, which cover basic operations such as arithmetic or storage functions. Complex functions can be integrated by using MegaCore functions in DSP Builder models.

See www.altera.com/dspbuilder for more details about Altera's DSP solutions.

FEATURES:

- Shortens DSP design cycles by linking MATLAB/Simulink tools with the Altera Quartus® II design software
- Fully supports Altera DSP IP
- Supports Stratix®, Stratix GX, Stratix II, Cyclone™, and Cyclone II FPGA families
- Enables rapid prototyping with Altera and third-party DSP development boards
- Hardware-in-the-Loop (HIL) block accelerates system-level co-simulation with Simulink and provides advanced debugging
- Supports the SignalTap® II logic analyzer in Altera's Quartus II software
- Offers customizable logic blocks for SOPC Builder system development tool and Nios® II embedded processor designs
- Includes state machine blocks, as well as Phase-Locked Loop (PLL) blocks for multi-clock designs
- Automatically generates a VHDL test bench or Quartus II Vector File (.vec) from MATLAB and Simulink test vectors
- Enables bit- and cycle-accurate design simulation
- Includes fixed-point arithmetic and logical operators for Simulink software

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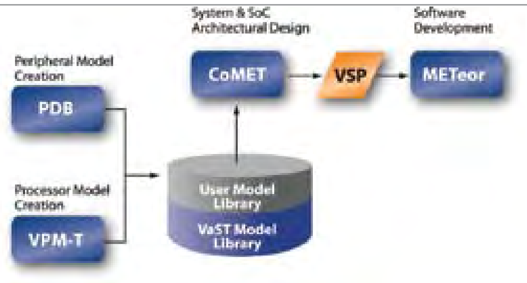
Virtual Prototype

VaST virtual system prototypes consist of fast, accurate, software tools and models for system-level engineering of SoCs and real-time and embedded systems. VaST provides CoMET, METeor, Peripheral Device Builder, and Metrix, plus fast and cycle-accurate models to make up a complete environment. CoMET and METeor enable architects, hardware designers, and software engineers to concurrently develop and verify their work. Metrix provides controllability and visibility of hardware and software execution far superior to that possible with hardware prototypes.

VaST supports many core processor and DSP models including the StarCore 1100, 2000, and 3000 families, as well as many standard and custom bus models. For more information, visit http://www.vastsystems.com.



FEATURES:

- A typical Virtual System Prototype consists of VaST models of multiple processors, complex buses, and peripheral devices
- VaST models run at speeds or 20-200 MIPS; timing accurate with cycle-by-cycle bus arbitration
- CoMET is the VaST tool used by architects and systems designers for architecture exploration and optimization
- Meteor is used by software developers in place of the actual hardware to design and integrate software

For more information, contact: l.prowsefosler@vastsystems.com RSC #6401 @ www.DSP-FPGA.com/catalogrsc

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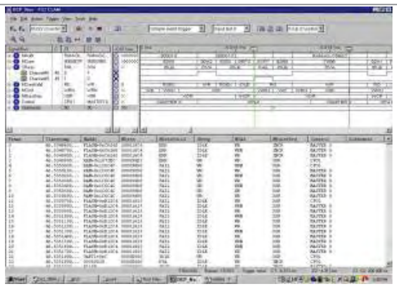
Bus Navigator

The FS2 Bus Navigator™ is used for monitoring signal activity and for debugging complex bus/system interactions in System-on-Chip designs. It allows the user to capture bus activity in real time and display critical information for analysis on a host PC. The system consists of an On-chip Instrumentation (OCI®) synthesizable logic block, a JTAG hardware probe, and PC-based software for controlling probing and analysis. The OCI passively captures bus activity, buffers it using on-chip RAM, and transfers the collected data off-chip via a JTAG port to the external JTAG probe.



FEATURES:

- Captures bus activity in real time
- Available for AMBA, OCP, Sonics Silicon Backplane, and custom buses
- Captures bus signals and user-defined inputs of other nodes
- Bus clock mode trace stores signals on every clock
- Bus transfer mode aligns bus transfers and response phases for single event triggering
- Easy-to-use graphical interface with state and waveform views

For more information, contact: info@fs2.com RSC #6402 @ www.DSP-FPGA.com/catalogrsc

Gedae, Inc.

Your Source for Embedded Signal Processing

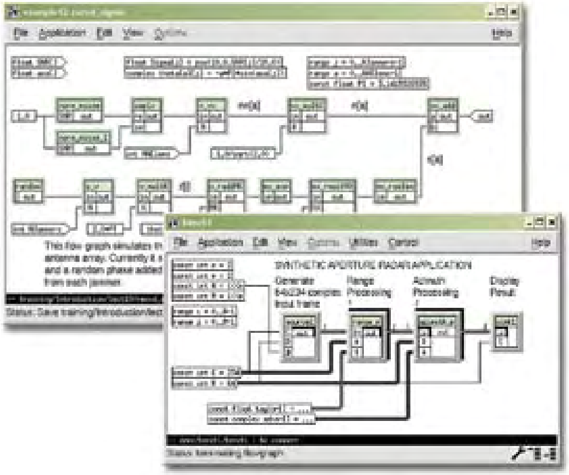
1247 N. Church Street
Moorestown, NJ 08057
Tel: 856-231-8783 • Fax: 856-231-1403
www.gedae.com

Gedae

Gedae 4.5

Gedae 4.5 is a software development tool for DSP and FPGA prototyping and implementation. It uses an easy-to-understand, block-diagram programming language to simplify development, reduce time to market, and cut life-cycle costs, while providing results that rival hand-coded quality but require dramatically less effort. Gedae automatically implements high-quality deployable DSP and FPGA software. After a developer designs and verifies the system software functionality on a workstation, Gedae implements the design by generating an application targeted to a specific embedded multiprocessor system. Gedae applies more than 100 algorithms to achieve the implementation, but the developer has complete control over it. The versatility of the tool makes it available for all aspects of development, including signal and data processing, application control, and integration with other systems. Gedae addresses the complete problem. Thus, Gedae avoids complex and costly interfaces between tools and the inefficiencies of mixed development methodologies associated with streaming data, granularity changes, dynamic data flow, distribution, and data transfers.

Gedae software supports development and distribution to multiple workstations or embedded processors. Applications include radar signal and data processing, mode control, and dynamic resource allocation; sonar signal and data processing mode control, adaptive algorithms, and application control; audio signal and data processing, interactive algorithms, and application control; image compression and classification; software radio communications; electro-optical signal and data processing, mode control, adaptive algorithms, and application control. Gedae is available for various COTS real-time embedded architectures from Bittware, Curtiss-Wright, Mercury, Motorola Systems, Sky, and VMETRO/Transtech.


File Application Edit View Options Help
File Application Edit View Options Utilities Control Help
SYNTHETIC APERTURE RADAR APPLICATION
Range Processing
Azimuth Processing
Display Result

FEATURES:

- Simplifies DSP and FPGA software prototyping and implementation
- Easy-to-use block diagram programming language
- Reduces time to market and cuts life-cycle costs
- Provides results that rival hand-coded quality
- Versatile enough for all aspects of DSP and FPGA development
- Applies more than 100 algorithms to achieve user-controlled implementation
- Eliminates complex and costly interfaces between tools
- Reduces inefficiencies caused by mixed development methodologies
- Supports multiple workstations or embedded processors
- Supports applications such as radar, sonar, imaging, radio, and electro-optics
- Available for several COTS real-time embedded architectures
- Board support package is available to support custom hardware and emerging technologies

For more information, contact: jlundgren@gedae.com

RSC #6501 @ www.DSP-FPGA.com/catalogrsc

RF Engines

Innovation Centre, St. Cross Business Park
Newport, Isle of Wight, PO30 5WB GB
Tel: +44-1983-550330 • Fax: +44-1983-550340
www.rfel.com

Your Source for Embedded Signal Processing

DSP Cores for FPGA

RFEL's signal processing cores are highly optimized FPGA designs for applications with high sample rates and demanding performance requirements. They provide a low-risk route for designers to exploit the full signal processing power of FPGAs. The designs can be targeted at Xilinx or Altera devices and are supported by bit-true MATLAB models.

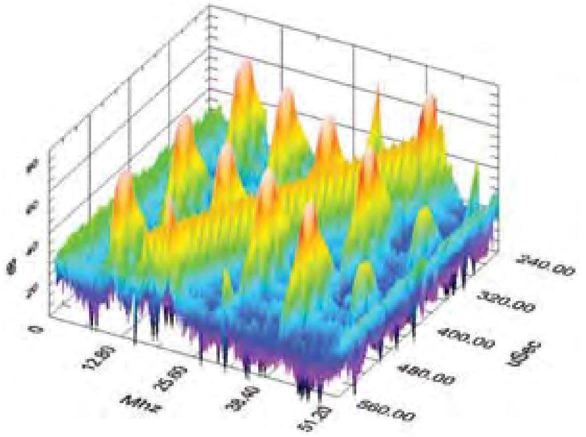
The FFT range includes the powerful HyperSpeed and HyperLength architectures, which support continuous complex sample rates up to 3.2 GHz or transform lengths up to 256 M complex points on a single FPGA. These architectures can also be customized for non-power-of-two transform sizes to exactly match the number of points required by the application. For less demanding requirements, RFEL also provides their Xilinx FFT library, which includes more than 60 highly optimized designs for complex sample rates up to 500 MHz and lengths up to 32 K points.

Polyphase DFT cores provide an efficient way to implement a uniformly distributed multichannel filter bank. This approach is generally used in applications that demand high-quality filters (frequency-bins) in terms of stop-band rejection and filter shape, and surpasses standard FFT windowing methods.

ChannelCore64 is RFEL's latest core for high-speed down-conversion. This core can extract up to 64 channels from two ADC inputs and enables the center frequency, bandwidth, and output sample rate to be set independently for each channel. The design is a flexible replacement for DDC ASICs in multichannel SDR applications, and variants are available on request.

All architectures can be quickly customized to meet specific performance requirements, ensuring the most silicon efficient solution. Furthermore, the company can provide a full design service to analyze requirements and develop and supply a complete FPGA-based system.

These products are just a selection of the cores in our signal processing range. Refer to our website for more details.



FEATURES:

- Guaranteed bit-true models provided with each core
- Highly optimized implementations using pipelined architectures
- Designs tailored to specific bit width and precision requirements
- Targeted at Xilinx and Altera FPGA devices
- Most design options already routed and proven on hardware
- Down-converter designs are cost-effective replacements for DDC hardware
- Full system design and consultancy service available
- Many applications in defense, instrumentation, telecom, and SDR
- Board independent designs
- Standard cores available off-the-shelf
- Many signal processing functions and interface cores available

For more information, contact: info@rfel.com

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Xilinx

2100 Logic Drive
San Jose, CA 95124
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www.xilinx.com/dsp

FPGA-DSP Tools

The XtremeDSP solution from Xilinx features the industry's most comprehensive suite of development tools to help you finish faster. Xilinx offers algorithms, design tools, multiple development platforms, and award-winning technical support.

Xilinx System Generator for DSP System Generator is the industry's preferred for developing DSP onto FPGAs. The tool enables you to model, design, simulate, verify, and debug your FPGA-based DSP system, even if you don't write a word of VHDL or Verilog.

Model and design: Your system may contain FPGAs and DSPs in the signal chain. Model the entire system using Simulink and blocksets from the The MathWorks. Design the FPGA section using the bit and cycle accurate Xilinx blockset.

Import MATLAB algorithms: Control algorithms can be imported directly into System Generator. For complex functions like linear algebra or matrix multiplies, import synthesized code from the Accelchip tool.

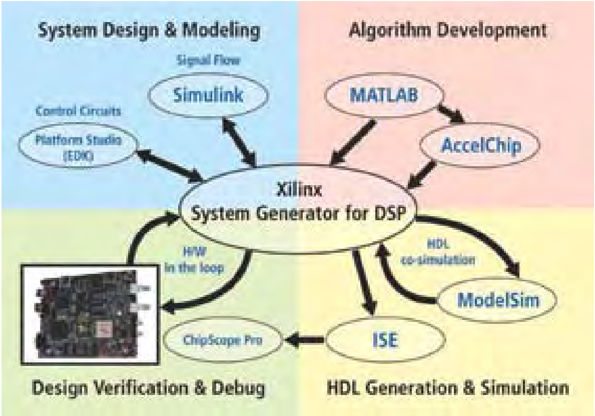
Simulaton and automatic HDL generation: Simulate your design in Simulink. You can also import legacy HDL code via a black box and simulate it in the loop using Model Sim. When done, System Generator will automatically generate efficient HDL, or a netlist or a bit-stream at the push of a button.

Verification and debug: Verify your system on your target hardware using our high-bandwidth hardware-in-the-loop (aka emulation) capability. Chip-scope probes can be used to monitor the FPGA's internal nodes to reduce debug time.

XtremeDSP algorithms
There are more than 60 DSP algorithms available from Xilinx and partners Examples include Viterbi decoders, RACH designs for 3G systems, filters, FFTs, etc.

XtremeDSP development platforms
Choose from one of multiple XtremeDSP development platforms for standalone or DSP-coprocessing designs from Xilinx or partners such as Lyrtech, Nallatech or Sundance.

Award-winning technical support
Count on our technical staff when you need it most to finish faster.



FEATURES:

- Model and design your system using MATLAB, Simulink, and blocksets from The MathWorks
- Use the Xilinx bit and cycle accurate library for designing the FPGA
- Import MATLAB algorithms like linear algebra and matrix inversion and multiplication
- Automatically generate HDL or a bitstream at the push of a button with no loss in performance over designs written in HDL
- Verify your system using hardware-in-the-loop (aka emulation); use chip-scope probes to speed up debug
- Choose from more than 60 XtremeDSP algorithms delivered as IP cores
- Choose from multiple XtremeDSP development platforms for video, digital communications or military applications like SDR and JTRS
- Use our field DSP specialists or award-winning technical support
- Learn about our Virtex-4 and Sparten 3/3E FPGAs for DSP; see the FPGA section
- Xilinx XtremeDSP education classes to help you finish faster

For more information, contact: narinder.lall@xilinx.com

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Acoustic Technologies

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Mesa, AZ 85204
Tel: 480-507-4376 • Fax: 480-507-4399
www.acoustictech.com

SoundClear Spkrphn

SoundClear speakerphone software enables natural conversation flow through echo cancellation, noise reduction, and sound enhancement along with sophisticated monitoring and control algorithms. This hands-free speakerphone software enables full-duplex communication and improves sound quality in mobile phones, VoIP phones, and other telephony products. The software is portable to many DSP architectures and is optimized for high-quality voice solutions with minimal MIPS and memory usage.

SoundClear software adapts quickly to changing environments and enables a natural conversation flow, just like a face-to-face conversation.

FEATURES:

- Full-duplex, natural flowing communication
- Voice-band graphic equalizers and speech emphasis
- Echo rejection of more than 42 dB, and noise cancellation up to 18 dB
- Adapts quickly to changing environments and noise
- Ideal for 3G videoconferencing and VoIP speakerphones
- Compliant with 3GPP, G.167, and G.168 standards

For more information, contact: sales@acoustictech.com RSC #6801 @ www.DSP-FPGA.com/catalogrsc

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Telecom software

Speech codecs & vocoders
ITU-T speech codecs (G.7xx) and proprietary low bit-rate vocoders (1200-8000 bps)

RealDuplex™
Full duplex echo cancellation integrated with noise suppression for reliable performance in any acoustic environment

G3/Super G3 fax bundle

- IITU-T V17, V27ter, V29, V21, V34 fax data pumps with G3 fax logic according to T30 solutions for high speed (up to 12800 bps) data/voice communication over HF channels in accordance with military standards and STANAG
- Highly sophisticated GPS receivers (up to 36 channels) based on TI DSP chips with proprietary software

FEATURES:

- Field-proven software (powers 50+ million voice channels globally)
- First-class tech support for easy integration and fast time to market
- Software tailored to meet customers' requirements for MIPS, memory, and target hardware limitations
- Wide experience (250+ projects successfully implemented during the last 12 years) and qualified technical team of 80 engineers
- Deeply optimized for the TI DSP platforms and can be ported to any other DSP or PC platform on request

For more information, contact: biz@spiritdsp.com RSC #6802 @ www.DSP-FPGA.com/catalogrsc

Synplicity, Inc.

600 W. California Avenue
Sunnyvale, CA 94086
Tel: 408-215-6000 • Fax: 408-222-0268
www.synplicity.com

Synplicity
Simply Better Results

Synplify® DSP

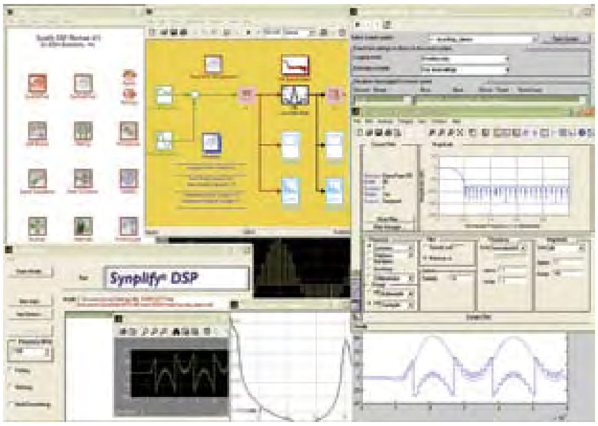
DSP designers are increasingly targeting FPGA hardware for implementation of their high-performance DSP designs. Today's FPGAs also contain large quantities of DSP blocks and multipliers facilitating efficient and parallel implementation of DSP functions in programmable logic. Until now, however, there has been no good way to get a design specified at the algorithm level from tools such as Simulink by The MathWorks into high-quality RTL code.

Synplify DSP software is a true DSP synthesis tool and the only one that performs high-level DSP optimizations from a Simulink specification. These special DSP optimizations enable designers to capture the behavior needed for their DSP algorithm without worrying about the specific implementation in hardware. The Synplify DSP tool automatically produces a highly optimized, technology independent implementation of the design ready for RTL synthesis.

A key feature of the Synplify DSP solution is an associated architecture-independent, and vendor-independent blockset (library) for use with Simulink. In order to aid in the conversion of the initial floating-point representations into their fixed-point counterparts, each of these library elements supports automatic data type propagation. This means that the user need only specify the fixed-point data types (signed, unsigned, etc.), and bit-widths of selected signals and derived values will then automatically propagate throughout the design.

Unlike conventional IP solutions, this blockset maintains the entry point for the DSP architects at the pure algorithmic level. That is, users are not obliged to define any low-level implementation decisions; the only parameters that need to be specified at this level are high-level attributes such as filter coefficients and gain requirements.

Synplify DSP software also performs system-level optimization techniques such as retiming, resource allocation, scheduling (folding), multichannelization, and architectural selection.



FEATURES:

- Fully integrated into the popular Simuling environment with no additional learning curve
- Fully integrated Synplicity fixed-point blockset of common DSP functions
- Floating-point to fixed-point conversion and analysis
- Performs system-level optimization for improved performance with fewer resources and area/speed tradeoffs
- High-quality RTL code and testbench automatically created from Simulink specification
- Technology independence enables targeting any FPGA architecture from the same Simulink source

For more information, contact: info@synplicity.com

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Kane Computing Ltd

Your Source for Embedded Signal Processing

7 Theatre Court, London Road
Northwich, CW9 5HB GB
Tel: 01606-351006 • Fax: 01606-351007
www.kanecomputing.co.uk

Predator2 Emulator

The Predator-II combines the performance of a PCI emulator with the convenience of portable external emulators. The emulator uses the standard Texas Instruments unified drivers and is fully compatible with Code Composer Studio and all current Windows operating systems. Predator-II is based on the well proven Predator PCMCIA Emulator with improved driver circuits and a new PCMCIA to POD cable to provide greater reliability, low-voltage DSP support with automatic voltage detection circuitry, plus new indicator lights on the POD. Predator-II is the perfect choice for laptop users who are in need of faster program load performances.

FEATURES:

- Fast download speeds for debugging large applications
- Easy portability in the field
- Ideal for handling large programs
- No need for external power
- Operation/Diagnostics via POD LEDs
- PCI carrier card option enables the Predator-II to be used with desktop PCs

For more information, contact: sales@kanecomputing.com

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Traquair Data Systems, Inc.

Your Source for Embedded Signal Processing

114 Sheldon Road
Ithaca, NY 14850
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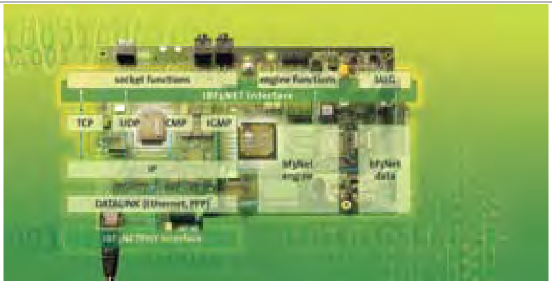
www.traquair.com

bf3Net

The bf3Net TCP/IP Protocol Stack by Windmill Innovations is a versatile, easy-to-use software package that enables Ethernet and Internet communications on a wide variety of TI DSP hardware platforms:

- Commercial off-the-shelf hardware (micro-line embedded DSP boards)
- Texas Instruments Development Starter Kits (DSKs)
- Custom-designed hardware incorporating TI DSPs

Customers can start developing with bf3Net on DSKs and micro-line embedded systems for as little as $995. A wide variety of upgrades are optionally available to expand bf3Net's capabilities, including a web server and application protocols such as POP3 and FTP.



FEATURES:

- eXpressDSP™-compliant TCP/IP protocol stack with integrated DMA support
- High communication efficiency and throughput
- Graphical development tools compliant with applicable Internet standards
- Modular, single-threaded architecture
- Integrated debug strategy
- Cross-platform independence

For more information, contact: sales@traquair.com

RSC #7002 @ www.DSP-FPGA.com/catalogrsc

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Stafford, TX. 77477 USA
Tel: 281.494.4500 x-113
Fax: 281.494.5310
www.spectrumdigital.com
sales@spectrumdigital.com
support.spectrumdigital.com

Spectrum Digital Emulators for TI DSPs

	XDS510PP PLUS JTAG	XDS510PP MPSD	SPI510 JTAG	SPI515 JTAG	SPI525 JTAG	SPI530 MPSD	XDS510USB JTAG
Part Number	701014	701041	701250	701515	701700	701121	701900
Price in USD	$1299.00	$ 1299.00	$ 2195.00	$ 1999.00	$ 2999.00	$ 2499.00	$ 1799.00
PC Interface	Parallel Port	Parallel Port	ISA	Parallel Port	PCI	Parallel Port	USB
TMS320C30-32		Yes				Yes	
TMS320VC33	Yes		Yes	Yes	Yes		Yes
TMS320C4x	Yes		Yes	Yes	Yes		Yes
TMS320C5x	Yes		Yes	Yes	Yes		Yes
TMS320F24x™	Yes		Yes	Yes	Yes		Yes
TMS320F240x	Yes		Yes	Yes	Yes		Yes
TMS320F28xx	Yes		Yes	Yes	Yes		Yes
TMS320C54x™	Yes		Yes	Yes	Yes		Yes
TMS320C55x™	Yes		Yes	Yes	Yes		Yes
TMS320C6xxx™	Yes		Yes	Yes	Yes		Yes
TMS320C64xx	Yes		Yes	Yes	Yes		Yes
TMS470 ARM7	Yes		Yes	Yes	Yes		Yes
TMS470 ARM9	Yes		Yes	Yes	Yes		Yes
OMAP	Yes		Yes	Yes	Yes		Yes
+3.3 to +5V	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1-5V (low power)			Yes	Yes	Yes		
1-5V with LVA	Yes						Yes
Supports CCS	Yes	Yes	Yes	Yes	Yes	Yes	Yes
SDFlash Spt	Yes		Yes	Yes	Yes		Yes

Emulator Accessories	Part Number	Price
Low Voltage Adapter for JTAG Emulators (LVA)	701208	$ 99.00
4 Channel JTAG Expander for JTAG Emulators	701204	$ 995.00
SPI110LV Optically Isolated Adapter for JTAG Emulators	701240	$ 1500.00

XDS510 USB with LVA

Prices shown here are valid for sales in the United States only. Foreign sales must be made through an agent or authorized reseller and prices may be different. All prices are your dock and are subject to change. Please contact Spectrum Digital for latest pricing and availability prior to ordering.

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Global IP Sound

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San Francisco, CA 94133
Tel: 415-397-2555 • Fax: 415-397-2577
www.globalipsound.com

GIPS VoiceEngine

GIPS VoiceEngine™ is a comprehensive, packaged solution that handles all the necessary voice components for VoIP, providing superior voice quality even under adverse network conditions. The patented solution consolidates all of the complex voice processing capabilities into a single solution to allow manufacturers to quickly and affordably integrate unmatched voice quality into their software solutions without in-house voice engineering expertise. The VoiceEngine product family includes VoiceEngine™ PC, VoiceEngine Mobile™, VoiceEngine Multimedia, and VoiceEngine Embedded. VoiceEngine supports existing standards and offers improved voice quality by the unique configuration of its components and by improved handling of the hardware.

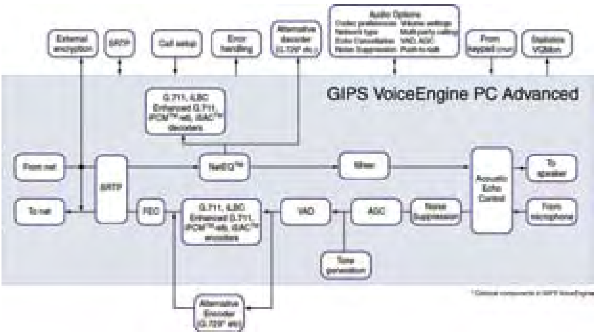
- Software plug-in with high-level API
- Real-time performance
- Complex speech enhancements, plus echo cancellation
- Multi-party calling with ad-hoc conferencing capabilities

GIPS VoiceEngine Embedded
VoiceEngine Embedded is an extension to the world-renowned GIPS VoiceEngine product family. GIPS VoiceEngine Embedded is designed for CPU-based VoIP equipment such as hardware IP phones or residential gateways – often referred to as Terminal Adaptors or IADs.

Accelerated time to market and reduced development costs
By leveraging Global IP Sound's patented solutions and expertise, developers and manufacturers are able to rapidly deploy voice-enabled products without having to solve the complex issues that affect voice quality.

Simplified integration of sound-processing software
Our solutions provide all the necessary interfaces and components to implement Voice over IP, allowing developers to focus on core competencies and product development rather than the complex integration and tuning of sound processing software.

Flexible and rich feature set
Global IP Sound provides comprehensive, best-of-breed solutions for use in products at all levels of the network architecture. Our solutions support existing standards, resulting in superior quality for all Voice over IP calls.



FEATURES:

- High-level API on all platforms
- Low latency and high packet loss robustness with GIPS NetEQ and GIPS codecs
- Narrowband and wideband codecs
- Forward Error Correction and RFC 2198
- VAD.DTX. CNG, speech level indicator, and microphone and speaker volume controls
- Acoustic echo cancellation and noise suppression
- Multi-party calling (between three and five callers)
- Video synchronization
- Compatible with any call setup protocol such as SIP and H323
- Push-to-talk, multichannel support
- RTCP and statistics
- Telchemy VQMon support

For more information, contact: info@globalipsound.com RSC #7201 @ www.DSP-FPGA.com/catalogrsc

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Your Source for Embedded Signal Processing

bf3Web

The bf3Web Embedded Webserver is Windmill Innovations' solution for creating web interfaces for DSP applications. Compatible with the bf3Net TCP/IP Protocol Stack, bf3Web provides the fastest way to develop websites hosted by a DSP system. The bf3Web Embedded Webserver is an HTTP 1.1-compliant server.

DSP application developers can start the design of their website using standard authoring tools such as Macromedia Dreamweaver. The bf3Web Integration Tool converts the pages and related files to C source and implements the file structure in the bf3Vfs Virtual File System. All source files are automatically added to the DSP project.

Support for Server-Side Includes and Common Gateway Interface scripts is also provided.

FEATURES:

- HTTP 1.1-compliant server
- Hierarchical directory structure for memory-based storage up to 65,534 files
- Directory-level user authentication with login and password for up to 16 users
- Graphical configuration and integration through bf3Vfs Integration Tool
- Integrated real-time clock for time stamping

For more information, contact: sales@traquair.com RSC #7301 @ www.DSP-FPGA.com/catalogrsc

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Understanding power efficiency in DSP applications

By Nat Seshan, PE, Distinguished Member Technical Staff
Advanced Architecture and Chip Technology Team
Digital Signal Processor Systems, Texas Instruments

DSP systems have long passed the point at which a single processing architecture can provide the best solution for all types of applications. Today, different architectures trade off performance, price, and power consumption – the "three Ps" –to optimize DSP products for different application areas. However, while the first two of these Ps secure a great deal of attention, the third secures less attention than it should. Concerning power consumption, developers often have little understanding of why one DSP may be better optimized for a specific application than another.

For many applications, power consumption can be just as significant an issue as performance, though it doesn't have the same glamour. Just as "miles per gallon" does not sound as sexy as horsepower or acceleration figures, milliwatts seem dull compared to MIPS and gigahertz. DSP vendors do not help clarify power consumption when they reduce it to a few published numbers that are often quoted for a non-typical operating temperature and with little relevance to the demands of the application. In the end, though, DSP power consumption is just as application-dependent as performance, and just as important for the designer to understand.

Power for different applications

DSPs and other processors consume power in three ways:

- Actively
- By clocking circuitry
- Through transistor leakage

Active power, which is consumed when the device is performing system operations, is addressed through efficient processing and I/O. Clocking power is directly proportional to the clock frequency of the device, offering the opportunity to reduce the overall power consumed through frequency modification. Leakage power, a constant drain on a device regardless of processing activity or operating frequency, depends on manufacturing processes for control. DSP manufacturing and design techniques address each of these areas to achieve the right mix of power consumption for the type of application.

Generally, where power efficiency is concerned, DSP applications fall into two groups: line-powered systems such as those used for communications infrastructure, and portable systems powered by batteries. The requirements of the first group tend to be dominated by performance considerations, but there are power constraints that cannot be ignored. For battery-operated applications, however, performance must always be evaluated in relation to how much power is consumed, so that power consumption is at least as important a design factor as execution speed. Portable applications are also more varied in their power requirements than plug-in systems.

Infrastructure systems

Even though communications infrastructure equipment such as Voice over Packet (VoP) systems or wireless base station transceivers are line-powered, they still operate under strict power constraints. Rack dimensions are usually fixed, as are the power supply and available cooling, so that a system that adds new processing functions or additional channel capacity must fit them into an existing space and operating environment. For the designer, the existing power supply imposes a power budget, which is divided among the various boards or "blades" in the rack, and that, in turn, among the board components. A related issue is the thermal budget, or how much heat dissipation the system can handle within its set space. Both the power and thermal budgets are "worst-case" constraints, and infrastructure equipments are designed to stay well within them.

DSPs used for infrastructure are designed to maximize performance while keeping power consumption within the required limits. Shrinking semiconductor geometries increase the frequency and processing efficiency of DSPs, allowing more channels to be handled by a single chip and more processors to be used in a given board area. The trade-off for this performance gain is that shrinking geometries causes increased power consumption over a reduced silicon area. Thus, it becomes increasingly important to dissipate heat efficiently through the IC package as well as the overall system. Since infrastructure equipments require the highest reliability, the power and thermal budgets must be observed even when all the processors are operating under maximum loading.

Battery-powered systems

Portable applications vary considerably in the way that they consume battery power. These products have unique operating mode profiles that require consideration, not only in optimizing the overall system, but also in optimizing the DSP architecture for the application. For example, an MP3 player consumes most of its battery power while it is playing songs, that is, in a mode of active operation. Standby time is limited, since the player usually shuts off automatically, and the player also spends relatively little time downloading songs. Since the main use of the DSP is for real-time decoding and decompressing of audio data, the device should operate with the greatest power efficiency in active operation and with a relatively light processing load.

> **"A DSP architecture can be tailor made to integrate the most power-efficient mix of peripherals and memory for a specific application."**

In contrast with the simple power profile of the MP3 player, a Digital Still Camera (DSC) has a complex profile, employing multiple operating modes that include capture and playback of still pictures, preview, standby, and sometimes video capture and playback. Capturing a still picture involves compressing and storing the image, while playback involves retrieving and decompressing the image before displaying it. Preview displays the image before it is captured, and standby may turn the display off before it ultimately turns off the camera. Video is similar to still capture and display, except that a stream of images may require a different compression algorithm. To satisfy the camera's real-time requirements, the DSP must be able to continuously display new images in preview mode, compress captured images in the shortest possible time to minimize shot-to-shot delay, and perhaps compress video images at an acceptable frame rate. Most of the various DSC modes consume power during active use of the camera, but they may not require the DSP to use all of its capabilities at all times. Therefore, the DSP should not only process imaging algorithms efficiently, but also operate as power-efficiently as possible during each of the DSC modes.

A wireless phone contrasts with both the MP3 player and the DSC in that it spends a great deal of time in standby mode, when the system is waiting for a call, as well as in active mode, when it is transmitting and receiving a call. The DSP should minimize leakage current during standby mode and use power efficiently during calls. Many new wireless phones are hybrid devices, integrating DSCs, MP3 players, Personal Digital Assistants (PDAs), and even video capabilities in the same unit with the phone. These additions complicate the operating modes of the system and may be best addressed through a heterogeneous architecture that includes more than one processing element. Whatever the processor's design, though, it must provide the means for the system to operate as power-efficiently as possible in all modes.

Techniques for optimizing power

DSP manufacturers have a number of techniques available to optimize power consumption for the different requirements of infrastructure and portable applications. The manufacturing process is tunable for operation at different voltage levels, and for transistors to switch at different transition voltages. Scaling operating voltage and clock frequency either statically or dynamically is possible, as well as establishing voltage and clock domains for powering on or clocking chip functions as needed. A DSP architecture can be tailor made to integrate the most power-efficient mix of peripherals and memory for a specific application. The processing device can also address other types of operations power-efficiently by integrating multiple processing elements, including DSP and RISC cores, as well as dedicated coprocessing engines.

Each process node or geometry can be optimized for operation at more than 1 V, providing different trade-offs of performance and power consumption. Transistors at a higher voltage more effectively clamp leakage current, while those at a lower voltage swing faster between states,

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Number of DSPs to achieve 600 MHz C55x MHz	2	3
Resulting total power for 600 MHz	600 mW	1050 mW

Table 1

supporting higher frequencies and increased performance. For instance, DSPs based on Texas Instruments' 130 nm CMOS process can operate at 1.6 V with nearly no leakage (like the TMS320C5509A), or at 1.2 V (such as the TMS320C5502) and nearly twice the frequency of 1.5x or more that of the higher voltage, though with a higher leakage current as well (refer to Table 1). For a cell phone, the higher voltage option is preferable, since the DSP will drain almost no battery power during long idle periods. On the other hand, the lower voltage option is better optimized for an infrastructure system, since the DSP may be able to perform more operations using a higher frequency. Additionally, since power scales geometrically with the voltage, the active power consumption is more favorable in the lower voltage device: 1.2 V is 25 percent less than 1.6 V, but (1.2 V/1.6 V)^2 reduces the active power consumed by 44 percent. In an infrastructure system, this ratio translates into more work that can be performed within the power and thermal budgets.

Even within the same voltage option of a process, transistors can be designed for different switching threshold voltages (V_T). A transistor with a low V_T switches faster, while one with a high V_T clamps leakage current more effectively. A single DSP can be designed with mostly high-V_T transistors except in speed-critical paths, where it uses low V_T transistors. This technique is valuable in lowering power consumption in all DSPs, regardless of the operating voltage and intended application.

> **"Ultimately, when selecting a DSP, understanding the power requirements of the application as well as what makes a given device power-efficient, and under what conditions it offers the best power optimization is of great benefit to the developer."**

Varying the voltage

In newer DSPs that have been designed for portable applications, a number of power-saving techniques have been developed by introducing variability into the operating voltage and frequency of the device. When the full performance of the device is not required by a given system, the DSP can be scaled statically to run at a lower voltage and frequency. Since power consumption decreases geometrically with the voltage and linearly with frequency, a DSP that operates at 1.1 V and 600 MHz consumes (1.1/1.2)^2 * (600/720), or about 70 percent of the active power consumed by the same device operating at 1.2 V and 720 MHz. Voltage and frequency can also be scaled dynamically, so that they are lowered during periods when the processor is lightly loaded, then raised again when the load is high. This technique requires hardware and software control mechanisms, but it can be a highly effective way of reducing power consumption in portable applications.

In addition, a DSP can be designed with multiple voltage domains, so different portions of the chip operate at different voltages, depending on performance requirements. Voltage domains require isolation circuits for protection, as well as translation circuitry for signal transfers across domains. Since internal voltage regulation is inefficient in high-performance digital processes, there needs to be support from multiple power supplies at the board level. A technique that is somewhat easier to implement is gating the on-chip power supply to enable power-down of portions of the DSP when they are not in use. Because of the isolation required, power supply gating has to be coarse-grained, operating at the module level rather than on individual circuits.

Varying the frequency

In newer DSPs that have been designed for portable applications, a number of power-saving techniques have been developed by introducing variability into the operating voltage and frequency of the device. When the full performance of the device is not required by a given system, the DSP can be scaled statically to run at a lower voltage and frequency. Since power consumption decreases geometrically with the voltage and linearly with frequency, a DSP that operates at 1.1 V and 600 MHz consumes (1.1/1.2)2 * (600/720), or about 70 percent (or about 84 percent per MHz) of the active power consumed by the same device operating at 1.2 V and 720 MHz (see Table 2). Voltage and frequency can

Frequency (MHz)	Voltage (V)	Relative Performance	Relative Active Power per MHz	Relative Leakage Power
720	1.2	100%	100%	100%
600	1.1	84%	84%	84%

Table 2

also be scaled dynamically, so that they are lowered during periods when the processor is lightly loaded, then raised again when the load is high. This technique requires hardware and software control mechanisms, but it can be a highly effective way of reducing power consumption in portable applications.

A clock domain can also be scaled dynamically if the loading changes over time. A function that operates with half its load for a period of time can be scaled back to half the frequency, saving half the active power consumed until the loading increases again and the higher frequency is resumed. Moreover, if a circuit remains unused for a period, clock gating enables it to remain unclocked or static until it is needed. Clock gating can be more fine-grained than power supply gating, so that the clock to individual circuits can be disabled. Clock-gated circuits can also "wake up" more quickly than powered-down functions, saving idle cycles. Control of clock gating is implemented through sleep modes that enable the user to disable portions of the device, and also through built-in logic that automatically controls the clock gates. An example of the latter is an Ethernet MAC that stays in sleep mode until activity is detected on the network, wakes to handle the transmission, then returns to sleep.

Power-conserving functionality

Well chosen on-chip functionality can also help reduce DSP power consumption. Today the heart of the device, and of the system as a whole, may consist of various types of processing elements, each optimized for specific operations. DSP cores are designed for the computation-intensive, real-time tasks involved in signal and image processing. General-Purpose Processor (GPP) cores such as ARM RISCs are better at handling tasks such as Graphical User Interfaces (GUI), network stacks, and overall system control. Both DSP and GPP cores are programmable, supporting the introduction of new algorithms or other software functionality.

In addition, special-purpose hardware coprocessors may be integrated to perform well defined functions as fast as possible for specific applications. For example, TI's TMS320C6416 DSP integrates Viterbi and Turbo coprocessorss for forward error correction in the 3G base station standard. Each type of processing element complements the others: a DSP would require more cycles to perform the tasks that are best performed by a GPP, and vice-versa, while a coprocessor cannot be adapted through programming. The result of integrating multiple processing elements is not only enhanced application performance, but also power savings over single-element implementations that are performing the same range of tasks.

Peripheral integration is highly dependent on the application, and the choice of the right on-chip peripherals can make a great difference in both performance and power consumption. For memory integration, the general rule is the more on-chip memory the better, up to the amount needed by the application. However, for memory-intensive applications such as video or imaging, integrating the required amount of SRAM for data may be cost-prohibitive compared to adding external DRAM. Similarly, multifunction systems might require a large amount of program memory that is infrequently accessed and does not need to be stored on-chip.

In these cases, a caching architecture can reduce the need for power-consuming accesses to external memory. Two-level caches bring the added benefit of reducing power consumption in on-chip memory as well. Small first-level (L1) memories for program and data that are directly connected to the DSP core cache the most frequently used portions of the main on-chip memory, which resides at a second level (L2) and serves as a cache for external memory. Compared to the L1 memories, L2 memory often runs slower and is organized using a larger, more power-optimized block. The majority of core accesses hit the L1s, which have less capacitance by virtue of being smaller than the L2, making them fast while reducing power consumption per access.

Understanding power consumption

Architectural techniques for optimizing power consumption are complex, and they require making tradeoffs that are difficult to evaluate from a few published numbers. Many DSPs are designed for use in specific application areas, helping system developers to focus on a few product offerings. In addition, some DSP vendors offer spreadsheets that allow the input of data concerning core loading, peripheral and memory utilization, and other factors to help developers more closely estimate the power requirements of a specific processor application.

Ultimately, when selecting a DSP, understanding the power requirements of the application as well as what makes a given device power-efficient, and under what conditions it offers the best power optimization is of great benefit to the developer. Infrastructure and portable applications use power differently, and there are marked differences among products in the latter group. Different DSPs make use of different process and architectural techniques to optimize power consumption, as well as performance and price, for target applications. Power efficiency may not sound as sexy as performance when it comes to promoting a DSP, but it can be just as important to understand.

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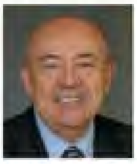

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COTS is the game, but is risk the same?

By Gerald A. Wilson, Ph.D., President and Founder, OmniSoft, Inc.

Using Commercial-Off-The-Shelf (COTS) hardware and software is the norm, rather than the exception it was years ago. Cost savings, both for initial procurement and long-term maintenance, are the clear objective. Hardware cost savings for acquisition are often significant. Software costs for COTS items, such as operating systems and utility libraries, may be higher initially, but lower for maintenance. More difficult to measure is the cost and schedule risk, both short- and long-term, of the project. Understanding and controlling risk is one of the most difficult challenges of using COTS hardware and software. If not properly addressed, the risk of COTS projects can be higher than projects using custom hardware and software.

Risk comes in many forms and different stages of a development effort. To a manager, risk represents the inability to meet contractual requirements, schedule delays, and cost overruns. To an engineer, risk is design failures that cause significant redesign, inadequate resources (people and/or equipment), requirements “creep” (such as changes in requirements after the project starts), and impenetrable technology barriers. During both development and deployed use, risk has a cumulative impact. Because risk is tricky to predict, it is often only recognized after-the-fact, when it is difficult, if not impossible, to control.

To illustrate how risk creeps into a project, consider a recent project to modernize a large military radar tracking system. The old system (excluding the radar antenna and power modules) used a number of custom digital processing boards and ASICs, and special-purpose processing algorithms. The new system uses a combination of COTS processors running a commercial OS (VxWorks in this case) and an FPGA module for special signal processing tasks. The radar display remains untouched. The control panels are Graphical User Interfaces (GUIs) on touch screens that maintain the look and feel of the original switches and buttons. This sounds like a well-defined and controlled custom-to-COTS upgrade with software maintainability benefits and low risk; in fact, that initial perception was far from reality.

There is little difference, from the risk perspective, between developing in DSPs, FPGAs, or conventional CPUs. Newer compilers hide much of the specialties of the hardware differences, and developers can often use C/C++ and other languages across all of these hardware environments. Testing is, of course, different, but the overall testing process is still the same: exercise all the modes and features in repeatable ways with measurements that clearly show compliance with requirements.

Purchasing an existing processor board has far lower risk than designing and fabricating a custom board, but there is risk. The COTS board will likely function differently from the custom board, and will require a change in the software. The FPGA board will require programming and will probably not function exactly like the custom circuits and ASICs. Other risk factors include:

1. “Fuzzy” requirements – New projects start by developing requirements. Because requirements are written documents but not usually implemented in prototypes, some details will be missed or ambiguous. With rework projects, such as the radar example described above, the original requirements documents may be out-of-date or missing.
2. Technology limitations – Custom designing the hardware and software for a project can minimize hardware limitations. COTS hardware/software comes with constraints imposed by the COTS design. These limitations can make writing the software more complicated. In addition, the requirements can be more difficult to achieve because there is less flexibility in the technology or less margin in computational power. COTS products rarely fit perfectly.
3. Nonoptimal choices – The COTS hardware with the best technology may be too expensive or may draw too much power. The COTS operating system best suited for the project/product may not be available for the selected COTS hardware. Pressure to make nonoptimal choices adds risk to the project.
4. Maintenance – Projects/products often have a useable life of 20 or more years. COTS hardware typically has support for only five to seven years. COTS software, however, may have a longer life span but tends to have new releases every year or so with older releases losing support. Companies providing COTS products may change or vanish throughout longer periods. The best technology choice may not be the best choice for maintenance and reliability, potentially putting the project at future risk.
5. Expertise – The experts who designed custom hardware are often available for advice if problems occur. With COTS hardware/software, the experts work for another organization, and their availability is limited at best.

> **"Managing risk in a COTS-based project requires attention to planning and risk mitigation strategies."**

The radar modernization project encountered all of these risks and more. Because the old system documentation was poor, many areas of the old system had to be reverse engineered to determine the actual requirements. Management selected a staff with inadequate experience and thus greatly extended the effort required. Inadequate testing facilities further delayed the project and forced testing and development on multiple shifts and weekends. Thus, the difficulty and cost of the effort had been significantly underestimated. The fault was not the use of COTS hardware/software but the incorrect assessment of the difficulty of the project. The project schedule ran more than twice as long as planned, and the costs were almost three times the initial proposal. With proper advice and controls, these risks would have been detected well before the project reached a crisis state.

Doesn't COTS reduce project risk? Using COTS reduces certain risks, but not all risks. COTS equipment and software reduces the risk and cost of custom development of hardware, operating systems, and tools by spreading that risk over a larger customer base. However, COTS will not improve the quality of the requirements specification or provide a better project plan and system design. When managers believe that COTS will enable successful completion of a project with fewer people and less experience, a project in trouble is often the result.

Managing risk in a COTS-based project requires attention to planning and risk mitigation strategies. The level of expertise required to successfully execute a COTS project is as high as or higher than that required for a fully custom hardware/software project.

For more information, visit the OmniSoft website at www.omnisoftinc.com.

Some steps for reducing/migrating your risk:

- **Do your homework early –** The initial design and background research needs to be done during the proposal phase if possible, or as the first activity of the project.
- **Seek outside comments –** Experts outside the project team who are familiar with the application area and the technology to be used should review the approach early.
- **Plan for the unexpected –** All projects have uncertainties. As knowledge improves, changes are likely to be required.
- **Have in-depth reviews often –** The situation will change, so periodic reviews of the design and the progress are essential.
- **Keep your customer involved –** What is opaque to you might be crystal clear to your customer if only you ask the correct question.
- **Don't fear change –** As problems arise, help the team think "out of the box" for solutions, rather than forcing adherence to an ill-fitting plan or approach.

Code generation and the complexity of applications

By William I. Lundgren, President, Gedae, Inc.

One of the trends in computing today is to provide ever more capable hardware platforms for the implementation of modern applications. However, more capable hardware is often more complex to program. Because of this complexity, software development is a key problem and major risk that confounds developers of digital systems. Not only is the development difficult the first time the system is implemented, but also each subsequent evolution in the hardware requires restructuring and rewriting of the underlying software.

Software layers and autocoding, two methods for tackling the issues of new, complex platforms, have different ways of helping developers meet the requirements of modern applications. In comparing the two methods, the separation of functionality and implementation, (for example, the separation between the description of the algorithms and the coding needed to port the algorithms to target hardware) is a significant differentiator, and autocoding proves to be the best approach.

Software layers and autocoding

Both software layers, a way of grouping functionalities at the same level of abstraction, and autocoding, the automatic generation of software from a partitioned and mapped data flow graph, allow a developer to work at a higher level of abstraction – more in the application functionality and less in the hardware. In the case of software layers, the hardware-specific implementation is buried underneath a common, hardware-independent interface.

For example, the Message Passing Interface (MPI) is a software layer that provides a standard interface across platforms for inter-processor communications, and the Vector Signal Image Processing Library (VSIPL) is a software layer that provides a standard interface across platforms for hardware-optimized vector routines for signal processing. These approaches work extremely well in low-level layers such as socket communications, but as the layers become deeper, the interface moves further away from the hardware, and the software becomes more complex and less efficient.

Autocoding is fundamentally different, as it automatically constructs the implementation. A developer specifies the application in a simple, high-level, hardware-independent language (often graphic-based), and the autocoding tool translates this specification to lower-level, hardware-specific code. Autocoding often relies on software layers to provide some of the hardware independence, but its true value is in its ability to tailor parts of the implementation directly to the hardware. If the tool merely changes the graphical representation into code that utilizes software layers, it does not qualify as a true autocoder. Autocoders in their purest form utilize complex algorithms that have fine control over the implementation using low-level, efficient software layers.

Comparing the two methods

The use of software layers meets some programming needs for implementation at a higher level of abstraction, resulting in productivity improvement as well as some level of increased portability. On the downside, software layers must have the capability to respond to widely varying needs of applications, often making them too complex to be efficient. In contrast, code generation can generate more of the application while minimizing the complexity of the implemented software.

For example, consider how both approaches implement inter-processor communications. When memory management is needed to perform a transfer, some software layer systems provide libraries that incur the overhead of managing memory, even when the memory allocations could be made ahead of time. Separate libraries – those with and without memory management – could eliminate the unnecessary overhead, but put the burden on the developer to choose the correct library and preplan the memory allocation.

On the other hand, an analysis-based autocoding system manages the entire implementation – not just the communication layer. This type of system can first peruse the functional specification and preplan the inter-processor communications to eliminate the overhead. Figure 1 represents the functional specification of an application, and separately, the implementation on a multiprocessor system. In the case shown, the transfers are moving data from data memory on the source processor directly into data memory on the destination processor.

Separation of functional description and implementation detail

In either development approach, if the functional description of the application is cluttered with implementation details, then portability will be limited. The key question is: What information is required in the functional description so that automatic implementation of efficient software is practical? While a paper description of a sensor system's functionality may be deemed sufficient information to generate an application, it does not provide practicality.

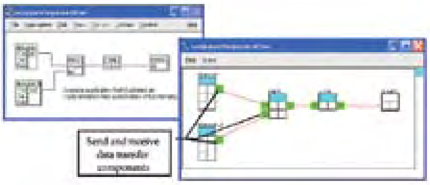

Figure 1

The focus has to be on providing information in a form that facilitates an implementation, while maximizing the quality of the implementation and minimizing the amount of implementation detail added to the functional description. While both software layers and autocoding provide this separation, autocoding provides a purer separation and better flexibility, which addresses the issues of software obsolescence and reduces implementation development time.

The addition of implementation to the functional description reduces portability because different architectures bring up different implementation issues. The implementation of an application on a shared memory architecture such as symmetric multiprocessing can be quite different from the implementation on a Direct Memory Access-based (DMA) architecture.

For example, in some systems, shared memory is not cacheable. In such a case, it is often important to get the data out of the shared memory at the first opportunity to avoid the execution inefficiencies. Although software layers can support such variations, either the layer is quite complex, giving rise to unnecessary overhead, or the developer must recognize the situation and make the necessary adjustments. With autocoding, the analysis and implementation routines can recognize the target-specific issues, and implement to accommodate and optimize for the various situations.

Analysis of implementation and reporting of runtime status

There is a wide range of code generation methods, but code generation has limited value if it is just the translation from one programming language to another with the insertion of large pieces of code. Instead, if there is an intermediate step in the code generation that forms an internal model of the software before outputting code, the model provides a method to analyze and optimize the generated implementation both more easily and in more fine detail. This level of analysis is unrealizable when using software layers alone.

Figure 2 illustrates the type of analysis that an autocoding tool can provide, given that it maintains an internal model of the software. Modern applications have dozens of components executing concurrently either as threads or on multiple processors, and the control necessary to operate these components can be very complex and can lead to difficult problems such as avoiding deadlock.

To illustrate one of these problems, Figure 2 creates a simple example with tokens dropped on one of the queues in order to artificially bring about a deadlock. In the block diagram of the functionality (bottom graph in the figure) data is being transferred down one path of processing that is calculating the average energy of the signal, and a primitive at the end of the branch is adjusting the average energy. In the implementation version of the block diagram (top graph in the figure), note the queues filled on one branch and starved on the other due to the dropping of tokens. The textual display describes the discovered problem, and the implementation display presents the information graphically. These capabilities are difficult to imagine in software libraries but are enabled by maintaining a software model in the development environment – something that is possible in an autocoding tool.

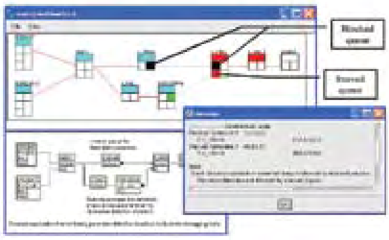

Figure 2

A winning solution for complex application development

A software tool that generates simple and efficient implementations can significantly reduce the issues associated with the growing complexity of application development. The issues associated with the practical separation of functionality and implementation need to be analyzed when generating code for complex hardware platforms. One autocoding tool, Gedae, is built based on the guiding principles to:

- Keep the functional specification free of implementation clutter
- Maintain a software model that is suitable for analysis and modification
- Autocode lean and efficient implementations

This type of tool helps developers more easily meet the requirements of modern applications.

For more information, visit the Gedae website at www.gedae.com.

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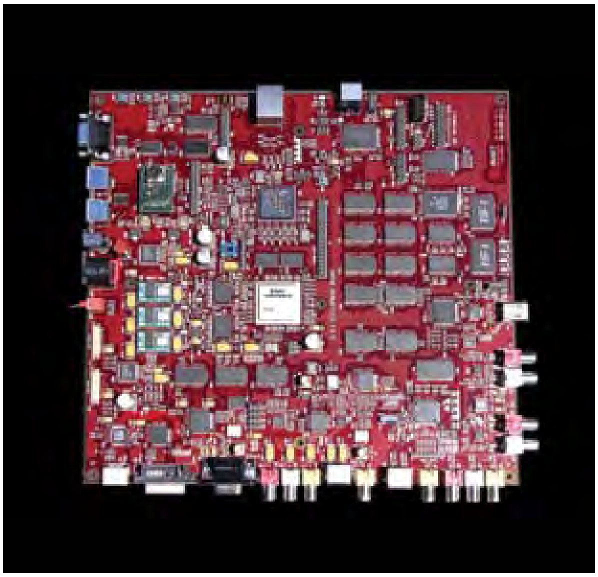
DSpXtreme Dev Kit

The DSpXtreme Development Board from Avnet Electronics Marketing combines a Texas Instruments® (TI) TMS320DM642 DSP and a Xilinx® Virtex- 4™ SX35 FPGA with a peripheral mix weighted toward multimedia and high-speed analog processing.

This combination provides a powerful mix of processing capability enabling the DSP and FPGA to operate as either standalone entities or cooperative entities with the FPGA providing high-speed repetitive type processing as a front- and/or back-end to the DSP. Application support is provided by 64 MB SDRAM (DSP), 128 MB DDR SDRAM (FPGA) and 64 MB of Flash memory. This module is powered for most applications by the included +5 V @ 4.5 A supply.

Interface description

- RS-232, PS2 keyboard/mouse
- 14-bit 125 MSps A/D converter
- 14-bit 165 MSps D/A converter
- DVI/HDMI
- USB 2.0
- IEEE1394
- Connector for Micron® MT9V022 VGA CMOS Image Sensor
- Connectors for STMicroelectronics® MOB-976/650-P01 1 Mpixel CMOS camera
- Connectors (2) for Sharp® LQ057Q3DC02 Color TFT LCD Module
- Connector for MPEG2 Transport Stream
- TI® TVP5600 Digital Video Decoder (480i/480p)
- TI® THS8200 RGB/Component Digital Video Encoder (480i/480p/720p/1080i/1080p)
- Philips® SAA7121H CVBY/YC Digital Video Encoder



FEATURES:

- TI® TMS320DM642 DSP (720 MHz)
- Xilinx® XC4VSX35-10FF668C
- Application support provided by 64 MB SDRAM (DSP), 128 MB DDR SDRAM (FPGA), and 64 MB of Flash Memory
- Connector for Micron® MT9V022 VGA CMOS Image Sensor
- Connectors for STMicroelectronics® MOB-976/650-P01 1 Mpixel CMOS camera
- Connectors (2) for Sharp® LQ057Q3DC02 Color TFT LCD Module
- TI® TVP5600 Digital Video Decoder (480i/480p)
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- Philips® SAA7121H CVBY/YC Digital Video Encoder
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For more information, contact: eval.kits@avnet.com

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4954-430 IP Core

The Pentek Model 4954-430 GateFlow Library IP Core is a 256-channel narrowband digital downconverter (DDC). Designed for use in Xilinx Virtex-II, Virtex-II Pro, and Virtex-4 FPGAs, Model 4954-430 utilizes a unique architecture to achieve 64 times the channel capacity of conventional quad ASIC downconverters. This Intellectual Property (IP) core is ideal for developers of applications requiring a high number of digital downconverter channels with size, weight, cost, and power constraints such as military radios and commercial wireless.

Accepting real or complex data at sample rates to 185 MHz, the architecture utilizes a channelizer stage that generates 1024 adjacent frequency channels with alias-free performance greater than 75 dB across the passband of each channel. A 256-position output switch matrix follows the channelizer, providing a coarse tuning capability for the desired output channels.

Each of the 256 DDCs has a programmable NCO (numerically controlled oscillator) to implement independent fine tuning for each channel and mixer, in order to translate the signal down to baseband. A decimating FIR low-pass filter follows and defines the channel bandwidth of the baseband output signal. The NCOs have a frequency tuning resolution of 32 bits and the baseband outputs pass through a programmable gain stage before rounded to a 16-bit result.

The decimation factor setting is common to all channels and is programmable from 1024 to 9984 in steps of 256. A factory default set of values is supplied: for an input sample rate of 185 MHz, the output bandwidth ranges from approximately 14.8 kHz to 144 kHz.

GateFlow IP Core 430 may be factory installed in the Pentek Model 7140 Digital Transceiver PMC/XMC module shown here, the Models 7240 and 7340 Digital Transceiver Compact PCI boards, and the Model 7640 Digital Transceiver PCI board.

For more information on the Model 4954-430 GateFlow IP Core, visit www.pentek.com/go/dsp430.

FEATURES:

- 256 channels of narrowband digital downconverter (DDC)
- Programmable number of individually tuned output channels up to 256
- Supports Virtex-II, Virtex-II Pro, and Virtex-4 FPGAs
- Extremely high channel-to-FPGA resource ratio
- Input data sample rates to 185 MHz
- Accepts 16-bit real or complex input data
- 256 fully programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation from 1024 to 9984 in steps of 256
- User-programmable 18-bit DDC FIR filter coefficients
- 75 dB stopband attenuation and 0.4 dB passband ripple (with default FIR coefficients)
- Downloadable simulation model available
- Test bench included

For more information, contact: info@pentek.com

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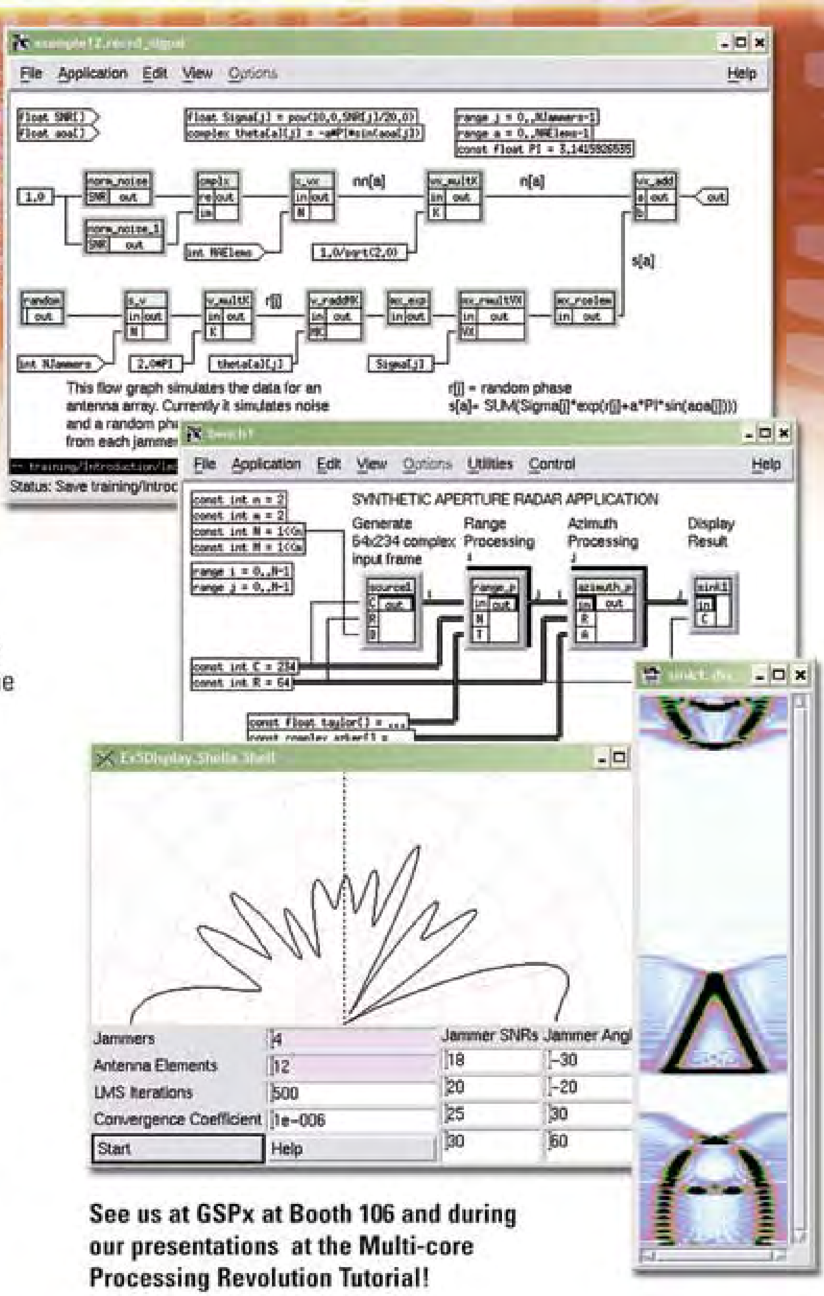
the Gedae approach to DSP/FPGA programming:

One picture is worth a thousand lines of code.

The Gedae software development tool for DSP and FPGA prototyping uses block diagram programming language to simplify development, reduce time-to-market, and cut life-cycle costs. You specify functionality through the block diagrams; Gedae's graphic diagnostic tools help you monitor implementation and performance throughout the process.

Gedae also creates a virtual machine environment, so complete systems can be developed independent of the target system. This highly optimized virtual machine provides efficiency rivaling that of hand-coded applications, with less development effort. And once your application is finalized, Gedae implements high-quality deployable software targeted to specific embedded hardware.

An additional advantage is the ease of accommodating inevitable changes at any point during the development or life cycle of a product. When you change implementation specifications, Gedae addresses all the complex issues associated with streaming data, dynamic data flow, distribution, and data transfers, completing the implementation within seconds. That's much easier than modifying C code, line by line.



This flow graph simulates the data for an antenna array. Currently it simulates noise and a random ph… from each jamme…

r[j] = random phase
s[a]= SUM(Sigma[j]*exp(r[j]+a*PI*sin(aoa[j])))

Status: Save training/Introd…

SYNTHETIC APERTURE RADAR APPLICATION

Generate 64x234 complex input frame
Range Processing
Azimuth Processing
Display Result

		Jammer SNRs	Jammer Angl
Jammers	4	18	-30
Antenna Elements	12	20	-20
LMS Iterations	500	25	30
Convergence Coefficient	1e-006	30	60

See us at GSPx at Booth 106 and during our presentations at the Multi-core Processing Revolution Tutorial!

Get the picture!
To appreciate how Gedae works, first hand, request a copy of our program demo CD by calling (856) 231-4458 or visiting ***www.gedae.com*** for a free download.

Gedae

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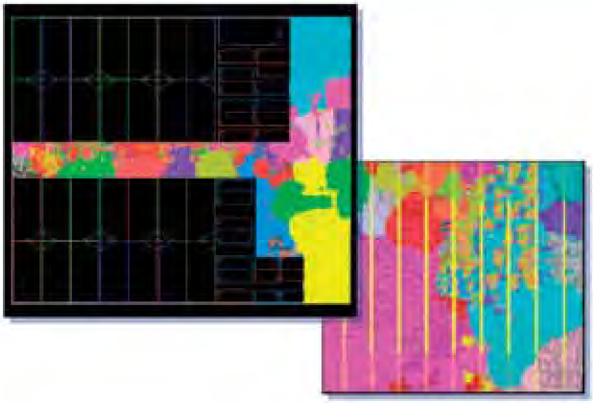

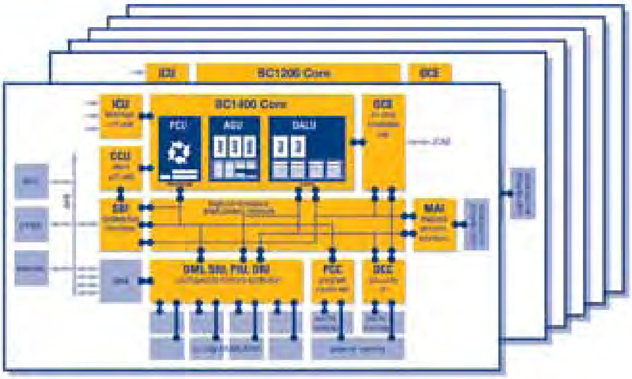

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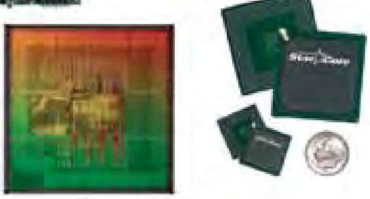

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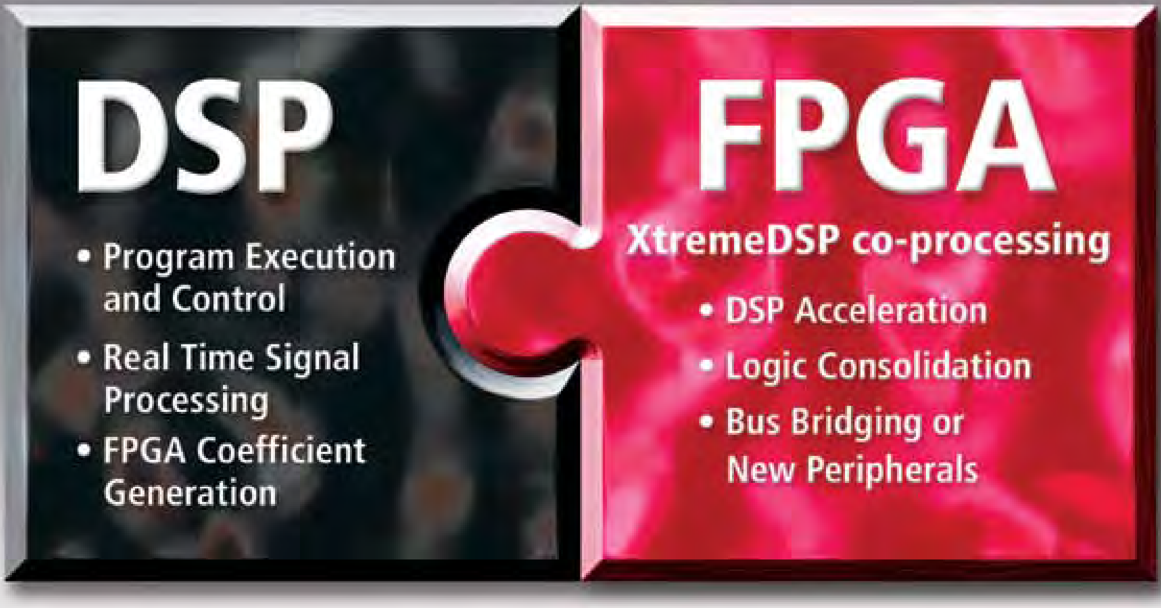
Turbocharge your DSP performance



DSP

- Program Execution and Control
- Real Time Signal Processing
- FPGA Coefficient Generation

FPGA

XtremeDSP co-processing

- DSP Acceleration
- Logic Consolidation
- Bus Bridging or New Peripherals

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